


Seed-Box

HINLINK			
Project:	HNAS	 HINLINK	
File:	01.Cover Page		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 1

Generate Bill of Materials

Header:

Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:

{Item}\{Value}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

Description

Note

Option

Notes

NOTE 1:


Component parameter description

1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

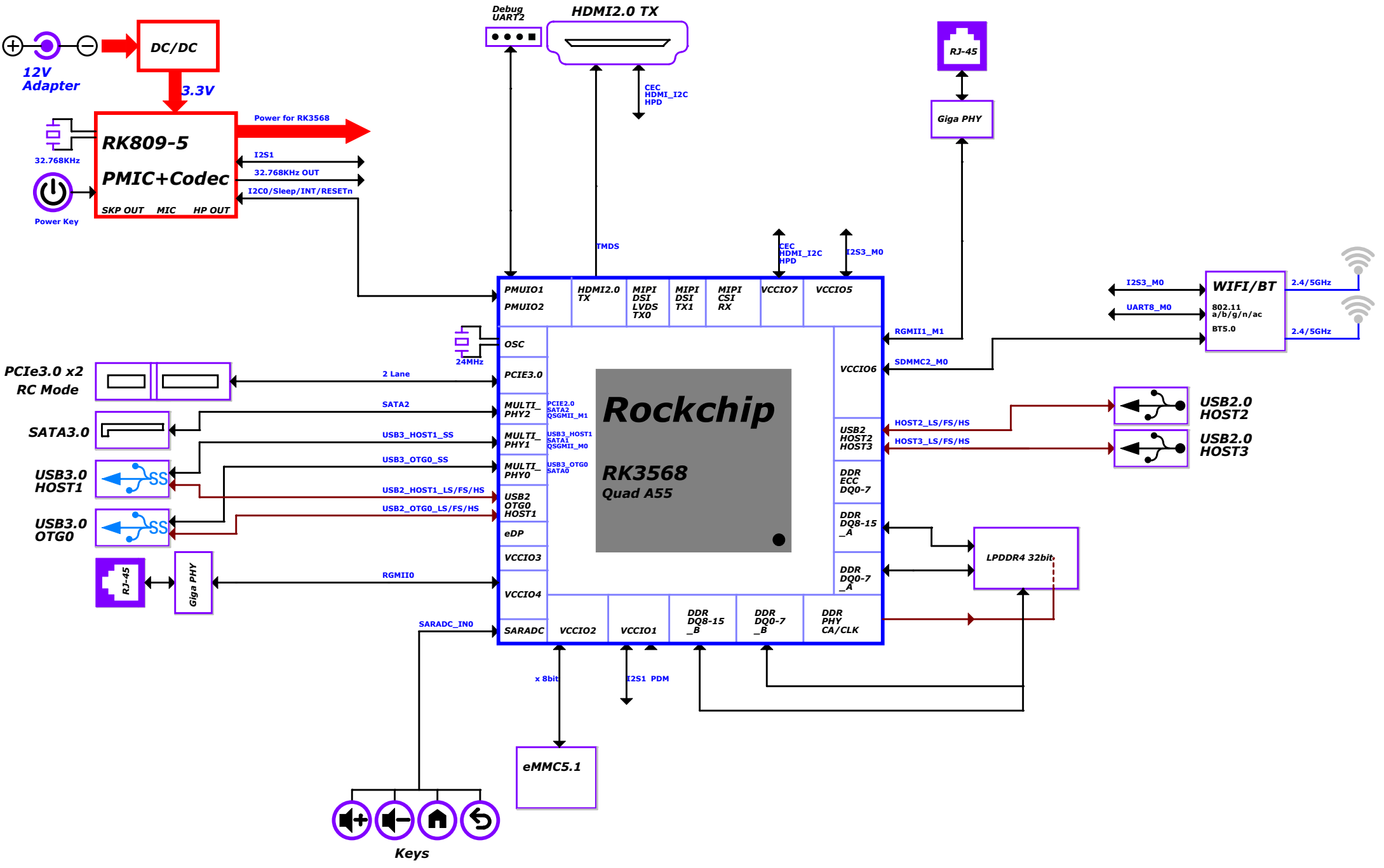
NOTE 2:

Please use our recommended components to avoid too many changes.
For more informations about the second source, please refer to our AVL.

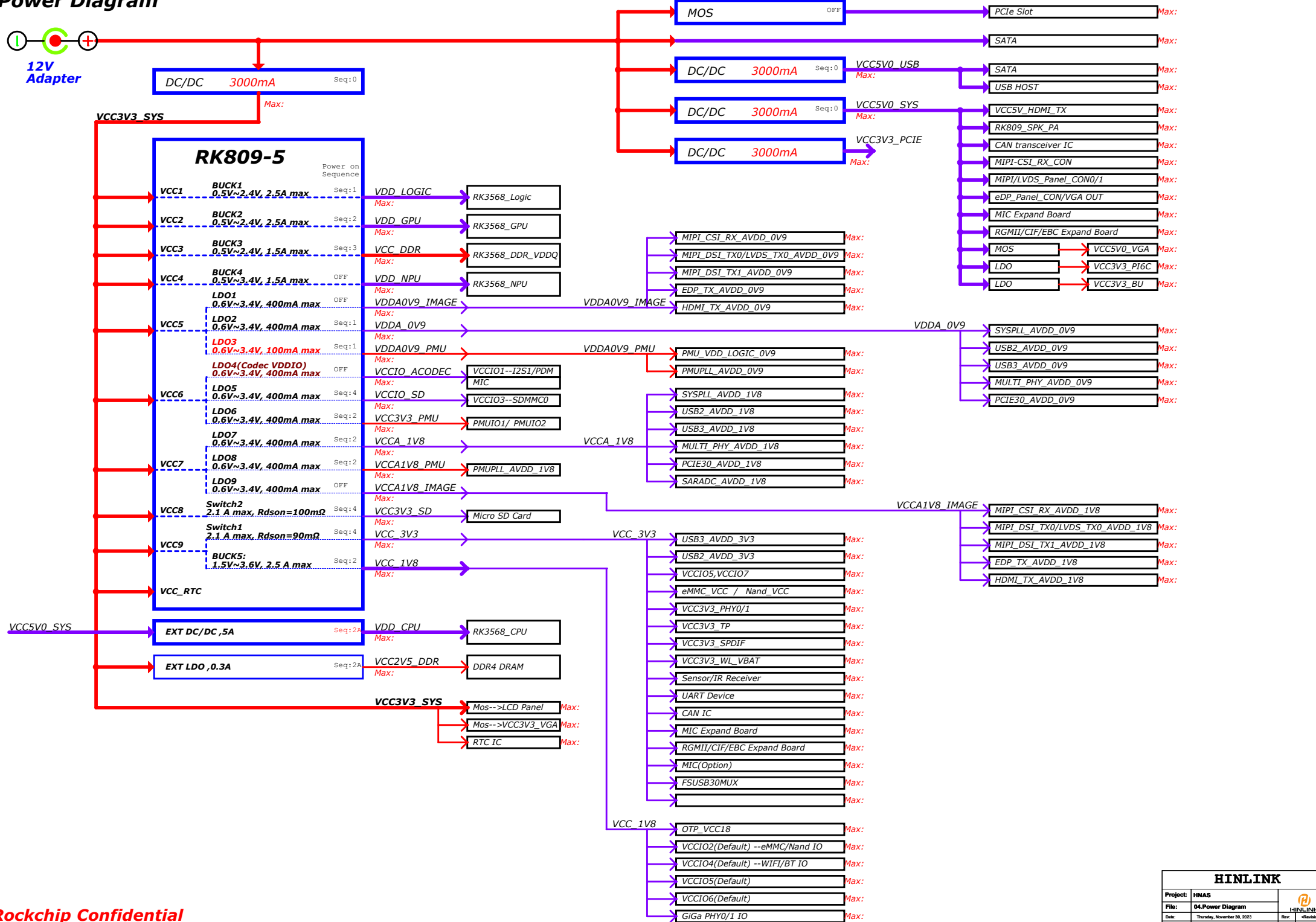
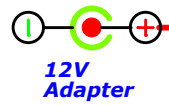
HINLINK

Project:	HNAS	 HINLINK	
File:	02.Index and Notes		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 2

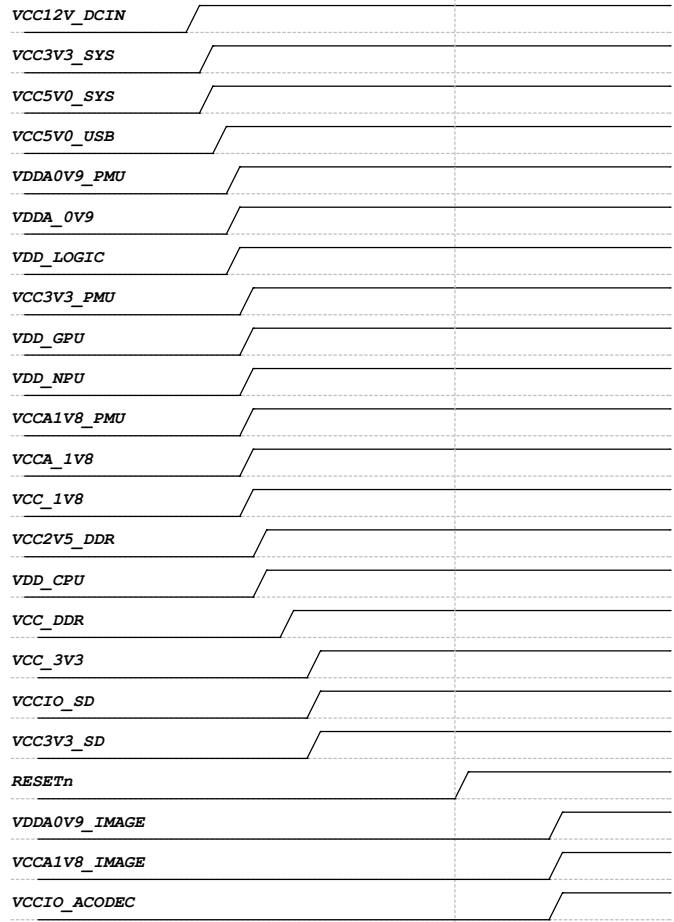
RK3568 Ref Block Diagram



Power Diagram



Power Sequence



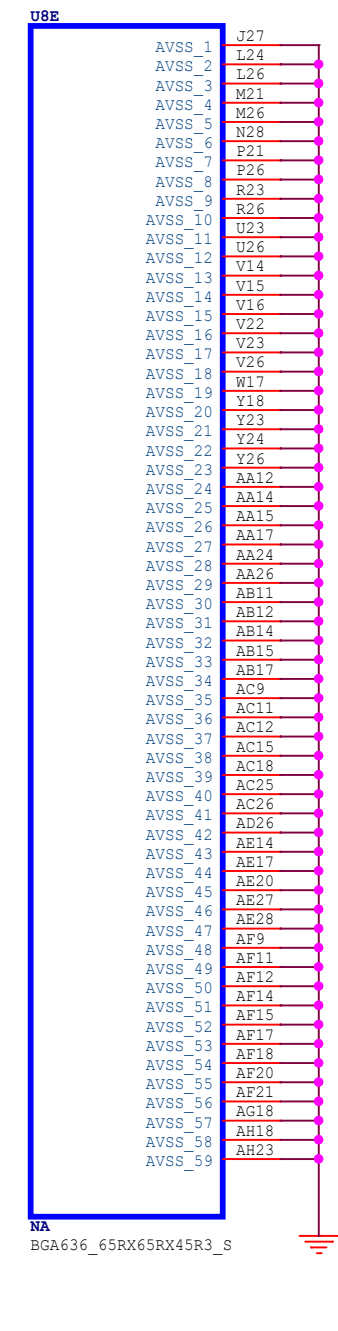
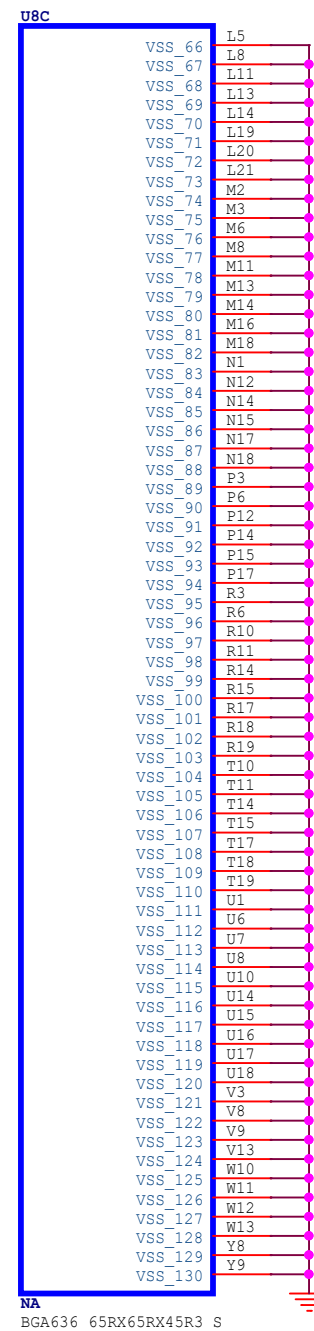
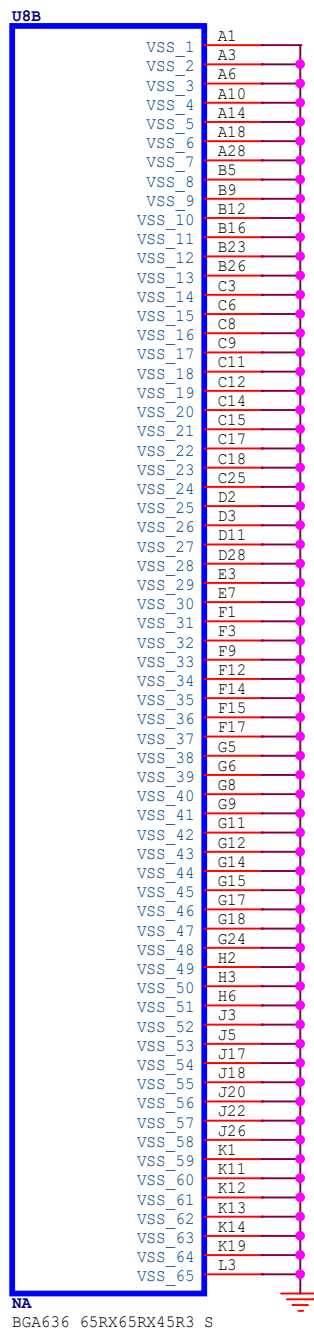
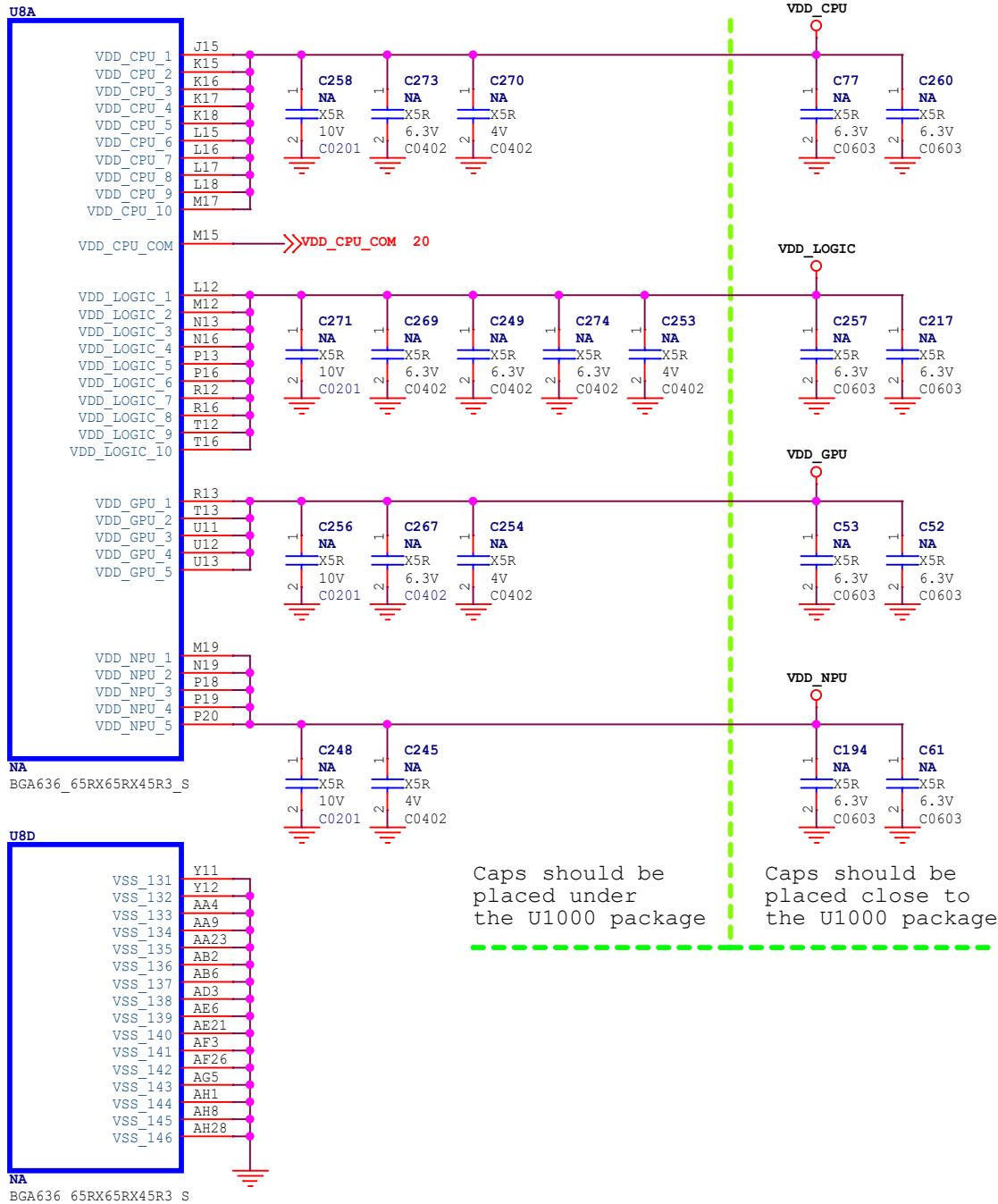
Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETh			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	ON	TBD	TBD


IO Power Domain Map

Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V, FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

RK3568_ABCDE (Power&Gnd)



HINLINK		
Project:	HNAS	 HINLINK
File:	06.RK3568_Power/GND	
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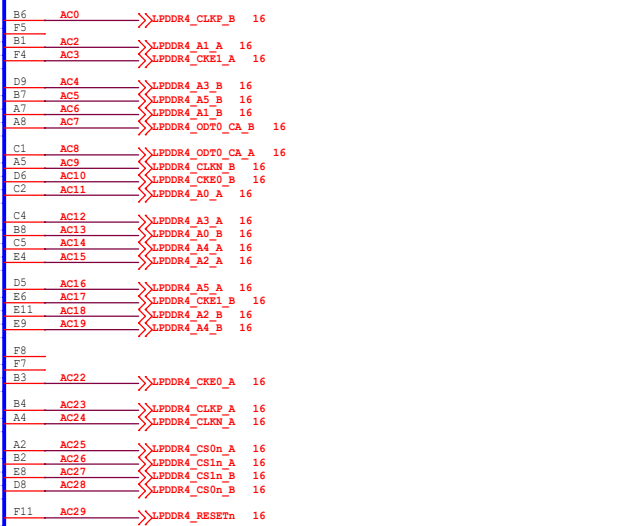
RK3568_F (DDR PHY)

UBF

	DDR4	LPDDR4	DDR3	LPDDR3	DDR4	LPDDR4	DDR3	LPDDR3
16 LPDDR4 DQ0 A	DDR DQ0 A	F2	DDR DQ0 A / DDR4 DQ0 A / LPDDR4 DQ0 A / DDR3 DQ0 / LPDDR3 DQ0	DDR4 A0 / LPDDR4 CLKP B / DDR3 A9 / --- / AC0	B6	AC0	LPDDR4 CLKP_B	16
16 LPDDR4 DQ1 A	DDR DQ1 A	E1	DDR DQ1 A / DDR4 DQ1 A / LPDDR4 DQ1 A / DDR3 DQ1 / LPDDR3 DQ1	DDR4 A1 / LPDDR4 CLKP B / DDR3 A9 / --- / AC0	F5	AC2	LPDDR4 AI_A	16
16 LPDDR4 DQ2 A	DDR DQ2 A	B2	DDR DQ2 A / DDR4 DQ2 A / LPDDR4 DQ2 A / DDR3 DQ2 / LPDDR3 DQ2	DDR4 A2 / LPDDR4 AI_A / DDR3 A9 / --- / AC0	B1	AC2	LPDDR4 AI_A	16
16 LPDDR4 DQ3 A	DDR DQ3 A	D1	DDR DQ3 A / DDR4 DQ3 A / LPDDR4 DQ3 A / DDR3 DQ3 / LPDDR3 DQ3	DDR4 A3 / LPDDR4 CKE1 A / DDR3 A9 / --- / AC0	F4	AC3	LPDDR4 CKE1_A	16
16 LPDDR4 DQ4 A	DDR DQ4 A	J1	DDR DQ4 A / DDR4 DQ4 A / LPDDR4 DQ4 A / DDR3 DQ4 / LPDDR3 DQ4	DDR4 A4 / LPDDR4 A3 B / DDR3 BA1 / LPDDR3 A3 / AC4	D9	AC4	LPDDR4 A3_B	16
16 LPDDR4 DQ5 A	DDR DQ5 A	J2	DDR DQ5 A / DDR4 DQ5 A / LPDDR4 DQ5 A / DDR3 DQ5 / LPDDR3 DQ5	DDR4 A5 / LPDDR4 A3 B / DDR3 BA1 / LPDDR3 A3 / AC4	B7	AC5	LPDDR4 A3_B	16
16 LPDDR4 DQ6 A	DDR DQ6 A	H1	DDR DQ6 A / DDR4 DQ6 A / LPDDR4 DQ6 A / DDR3 DQ6 / LPDDR3 DQ6	DDR4 A6 / LPDDR4 AI_A / DDR3 A9 / --- / AC0	A7	AC6	LPDDR4 AI_B	16
16 LPDDR4 DQ7 A	DDR DQ7 A	A4	DDR DQ7 A / DDR4 DQ7 A / LPDDR4 DQ7 A / DDR3 DQ7 / LPDDR3 DQ7	DDR4 A7 / LPDDR4 ODT0 CA B / DDR3 A9 / --- / AC0	A8	AC7	LPDDR4 ODT0_CA_B	16
16 LPDDR4 DM0 A	DDR DM0 A	H5	DDR DM0 A / DDR4 DM0 A / LPDDR4 DM0 A / DDR3 DM0 / LPDDR3 DM1	DDR4 A8 / LPDDR4 ODT0 CA A / DDR3 A6 / LPDDR3 A9 / AC8	C1	AC8	LPDDR4 ODT0_CA_A	16
16 LPDDR4 DQS0P A	DDR DQS0P A	G1	DDR DQS0P A / DDR4 DQSL P A / LPDDR4 DQS0P A / DDR3 DQS0P / LPDDR3 DQS1P	DDR4 A9 / LPDDR4 CLKN B / DDR3 A5 / --- / AC9	A5	AC9	LPDDR4 CLKN_B	16
16 LPDDR4 DQS0N A	DDR DQS0N A	G2	DDR DQS0N A / DDR4 DQSL N A / LPDDR4 DQS0N A / DDR3 DQS0N / LPDDR3 DQS1N	DDR4 A10 / LPDDR4 CKEO B / DDR3 A10 / --- / AC10	D6	AC10	LPDDR4 CKEO_B	16
16 LPDDR4 DQ8 A	DDR DQ8 A	M1	DDR DQ8 A / DDR4 DQ8 A / LPDDR4 DQ8 A / DDR3 DQ8 / LPDDR3 DQ8	DDR4 A11 / LPDDR4 AI_A / DDR3 A9 / --- / AC0	C2	AC11	LPDDR4 AI_A	16
16 LPDDR4 DQ9 A	DDR DQ9 A	N2	DDR DQ9 A / DDR4 DQ9 A / LPDDR4 DQ9 A / DDR3 DQ9 / LPDDR3 DQ9	DDR4 A12 / LPDDR4 A3 A / DDR3 BA2 / --- / AC12	C4	AC12	LPDDR4 A3_A	16
16 LPDDR4 DQ10 A	DDR DQ10 A	L7	DDR DQ10 A / DDR4 DQ10 A / LPDDR4 DQ10 A / DDR3 DQ10 / LPDDR3 DQ10	DDR4 A13 / LPDDR4 AI_A / DDR3 A9 / --- / AC0	B8	AC13	LPDDR4 AI_B	16
16 LPDDR4 DQ11 A	DDR DQ11 A	L6	DDR DQ11 A / DDR4 DQ11 A / LPDDR4 DQ11 A / DDR3 DQ11 / LPDDR3 DQ11	DDR4 A14 WEN / LPDDR4 A4 A / DDR3 A9 / --- / AC14	C5	AC14	LPDDR4 A4_A	16
16 LPDDR4 DQ12 A	DDR DQ12 A	K2	DDR DQ12 A / DDR4 DQ12 A / LPDDR4 DQ12 A / DDR3 DQ12 / LPDDR3 DQ12	DDR4 A15 CASn / LPDDR4 A2 A / DDR3 A0 / --- / AC15	E4	AC15	LPDDR4 A2_A	16
16 LPDDR4 DQ13 A	DDR DQ13 A	J6	DDR DQ13 A / DDR4 DQ13 A / LPDDR4 DQ13 A / DDR3 DQ13 / LPDDR3 DQ13	DDR4 A16 RASn / LPDDR4 A5 A / DDR3 BASn / LPDDR3 A7 / AC16	D5	AC16	LPDDR4 A5_A	16
16 LPDDR4 DQ14 A	DDR DQ14 A	U7	DDR DQ14 A / DDR4 DQ14 A / LPDDR4 DQ14 A / DDR3 DQ14 / LPDDR3 DQ14	DDR4 A17 / LPDDR4 CKE1 B / DDR3 A9 / --- / AC0	E6	AC17	LPDDR4 CKE1_B	16
16 LPDDR4 DQ15 A	DDR DQ15 A	L4	DDR DQ15 A / DDR4 DQ15 A / LPDDR4 DQ15 A / DDR3 DQ15 / LPDDR3 DQ15	DDR4 BA0 / LPDDR4 AI_A / DDR3 A9 / --- / AC0	E11	AC18	LPDDR4 AI_B	16
16 LPDDR4 DM1 A	DDR DM1 A	J4	DDR DM1 A / DDR4 DM1 A / LPDDR4 DM1 A / DDR3 DM1 / LPDDR3 DM1	DDR4 BA1 / LPDDR4 AI_A / DDR3 A9 / --- / AC0	E9	AC19	LPDDR4 AI_B	16
16 LPDDR4 DQS1P A	DDR DQS1P A	L2	DDR DQS1P A / DDR4 DQSU P A / LPDDR4 DQS1P A / DDR3 DQS1P / LPDDR3 DQS1P	DDR4 B0 / LPDDR4 ODT1 CA B / DDR3 WEN / --- / AC20	F8			
16 LPDDR4 DQS1N A	DDR DQS1N A	L1	DDR DQS1N A / DDR4 DQSU N A / LPDDR4 DQS1N A / DDR3 DQS1N / LPDDR3 DQS1N	DDR4 B1 / LPDDR4 ODT1 CA A / DDR3 BA0 / --- / AC21	F7			
16 LPDDR4 DQ0 B	DDR DQ0 B	B10	DDR DQ0 B / DDR4 DQ0 B / LPDDR4 DQ0 B / DDR3 DQ0 / LPDDR3 DQ0	DDR4 B2 / LPDDR4 CKEO A / DDR3 CKEO / LPDDR3 CKEO	B3	AC22	LPDDR4 CKEO_A	16
16 LPDDR4 DQ1 B	DDR DQ1 B	A9	DDR DQ1 B / DDR4 DQ1 B / LPDDR4 DQ1 B / DDR3 DQ1 / LPDDR3 DQ1	DDR4 CLKP / LPDDR4 CKEO A / DDR3 CKEO / LPDDR3 CKEO	B4	AC23	LPDDR4 CKEO_A	16
16 LPDDR4 DQ2 B	DDR DQ2 B	D12	DDR DQ2 B / DDR4 DQ2 B / LPDDR4 DQ2 B / DDR3 DQ2 / LPDDR3 DQ2	DDR4 CLKN / LPDDR4 CKEO A / DDR3 CKEO / LPDDR3 CKEO	A4	AC24	LPDDR4 CLKN_A	16
16 LPDDR4 DQ3 B	DDR DQ3 B	E12	DDR DQ3 B / DDR4 DQ3 B / LPDDR4 DQ3 B / DDR3 DQ3 / LPDDR3 DQ3	DDR4 C30n / LPDDR4 C30n A / DDR3 ODT1 / LPDDR3 ODT0 / AC25	A2	AC25	LPDDR4 C30n_A	16
16 LPDDR4 DQ4 B	DDR DQ4 B	A12	DDR DQ4 B / DDR4 DQ4 B / LPDDR4 DQ4 B / DDR3 DQ4 / LPDDR3 DQ4	DDR4 C50n / LPDDR4 C50n A / DDR3 ODT1 / LPDDR3 ODT0 / AC25	B2	AC26	LPDDR4 C50n_A	16
16 LPDDR4 DQ5 B	DDR DQ5 B	D15	DDR DQ5 B / DDR4 DQ5 B / LPDDR4 DQ5 B / DDR3 DQ5 / LPDDR3 DQ5	DDR4 CS0n / LPDDR4 CS0n A / DDR3 ODT1 / LPDDR3 ODT0 / AC25	E8	AC27	LPDDR4 CS0n_B	16
16 LPDDR4 DQ6 B	DDR DQ6 B	E15	DDR DQ6 B / DDR4 DQ6 B / LPDDR4 DQ6 B / DDR3 DQ6 / LPDDR3 DQ6	DDR4 CS0n / LPDDR4 CS0n A / DDR3 ODT1 / LPDDR3 ODT0 / AC25	D8	AC28	LPDDR4 CS0n_B	16
16 LPDDR4 DQ7 B	DDR DQ7 B	B14	DDR DQ7 B / DDR4 DQ7 B / LPDDR4 DQ7 B / DDR3 DQ7 / LPDDR3 DQ7	DDR4 RESETn / LPDDR4 RESETn / DDR3 BESETn / --- / AC29	F11	AC29	LPDDR4 RESETn	16
16 LPDDR4 DM0 B	DDR DM0 B	D14	DDR DM0 B / DDR4 DM0 B / LPDDR4 DM0 B / DDR3 DM0 / LPDDR3 DM0					
16 LPDDR4 DQS0P B	DDR DQS0P B	A11	DDR DQS0P B / DDR4 DQS0 P B / LPDDR4 DQS0P B / DDR3 DQS2P / LPDDR3 DQS0P					
16 LPDDR4 DQS0N B	DDR DQS0N B	B11	DDR DQS0N B / DDR4 DQS0 N B / LPDDR4 DQS0N B / DDR3 DQS2N / LPDDR3 DQS0N					
16 LPDDR4 DQ8 B	DDR DQ8 B	A16	DDR DQ8 B / DDR4 DQ8 B / LPDDR4 DQ8 B / DDR3 DQ8 / LPDDR3 DQ8					
16 LPDDR4 DQ9 B	DDR DQ9 B	B17	DDR DQ9 B / DDR4 DQ9 B / LPDDR4 DQ9 B / DDR3 DQ9 / LPDDR3 DQ9					
16 LPDDR4 DQ10 B	DDR DQ10 B	A17	DDR DQ10 B / DDR4 DQ10 B / LPDDR4 DQ10 B / DDR3 DQ10 / LPDDR3 DQ10					
16 LPDDR4 DQ11 B	DDR DQ11 B	B18	DDR DQ11 B / DDR4 DQ11 B / LPDDR4 DQ11 B / DDR3 DQ11 / LPDDR3 DQ11					
16 LPDDR4 DQ12 B	DDR DQ12 B	E13	DDR DQ12 B / DDR4 DQ12 B / LPDDR4 DQ12 B / DDR3 DQ12 / LPDDR3 DQ12					
16 LPDDR4 DQ13 B	DDR DQ13 B	A13	DDR DQ13 B / DDR4 DQ13 B / LPDDR4 DQ13 B / DDR3 DQ13 / LPDDR3 DQ13					
16 LPDDR4 DQ14 B	DDR DQ14 B	D17	DDR DQ14 B / DDR4 DQ14 B / LPDDR4 DQ14 B / DDR3 DQ14 / LPDDR3 DQ14					
16 LPDDR4 DQ15 B	DDR DQ15 B	B14	DDR DQ15 B / DDR4 DQ15 B / LPDDR4 DQ15 B / DDR3 DQ15 / LPDDR3 DQ15					
16 LPDDR4 DM1 B	DDR DM1 B	E17	DDR DM1 B / DDR4 DM1 B / LPDDR4 DM1 B / DDR3 DM1 / LPDDR3 DM1					
16 LPDDR4 DQS1P B	DDR DQS1P B	B15	DDR DQS1P B / DDR4 DQSL P B / LPDDR4 DQS1P B / DDR3 DQS3P / LPDDR3 DQS2P					
16 LPDDR4 DQS1N B	DDR DQS1N B	A15	DDR DQS1N B / DDR4 DQSL N B / LPDDR4 DQS1N B / DDR3 DQS3N / LPDDR3 DQS2N					
16 LPDDR4 ECC DQ0	DDR ECC DQ0	F2	DDR ECC DQ0 / DDR4 ECC DQ0 / --- / DDR3 ECC DQ0					
16 LPDDR4 ECC DQ1	DDR ECC DQ1	M4	DDR ECC DQ1 / DDR4 ECC DQ1 / --- / DDR3 ECC DQ1					
16 LPDDR4 ECC DQ2	DDR ECC DQ2	M5	DDR ECC DQ2 / DDR4 ECC DQ2 / --- / DDR3 ECC DQ2					
16 LPDDR4 ECC DQ3	DDR ECC DQ3	M7	DDR ECC DQ3 / DDR4 ECC DQ3 / --- / DDR3 ECC DQ3					
16 LPDDR4 ECC DQ4	DDR ECC DQ4	R7	DDR ECC DQ4 / DDR4 ECC DQ4 / --- / DDR3 ECC DQ4					
16 LPDDR4 ECC DQ5	DDR ECC DQ5	P4	DDR ECC DQ5 / DDR4 ECC DQ5 / --- / DDR3 ECC DQ5					
16 LPDDR4 ECC DQ6	DDR ECC DQ6	R4	DDR ECC DQ6 / DDR4 ECC DQ6 / --- / DDR3 ECC DQ6					
16 LPDDR4 ECC DQ7	DDR ECC DQ7	E7	DDR ECC DQ7 / DDR4 ECC DQ7 / --- / DDR3 ECC DQ7					
16 LPDDR4 ECC DM	DDR ECC DM	P2	DDR ECC DM / DDR4 ECC DM / --- / DDR3 ECC DM					
16 LPDDR4 ECC DQS P	DDR ECC DQS P	F1	DDR ECC DQS P / DDR4 ECC DQS P / --- / DDR3 ECC DQS P					
16 LPDDR4 ECC DQS N	DDR ECC DQS N	F1	DDR ECC DQS N / DDR4 ECC DQS N / --- / DDR3 ECC DQS N					

Note: Sequences can not be swap

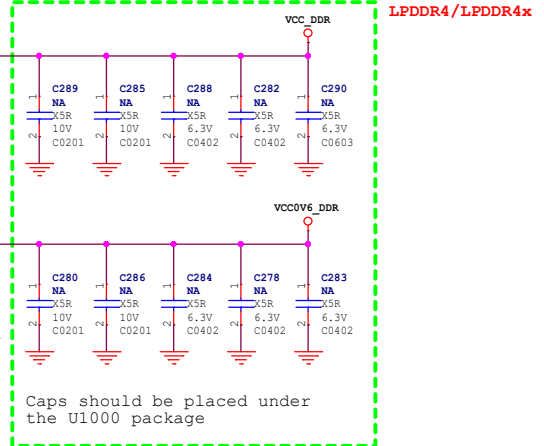
Note: Except DDR3, other DQ sequences can not be swap



For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RQ pin and VDDQ pin

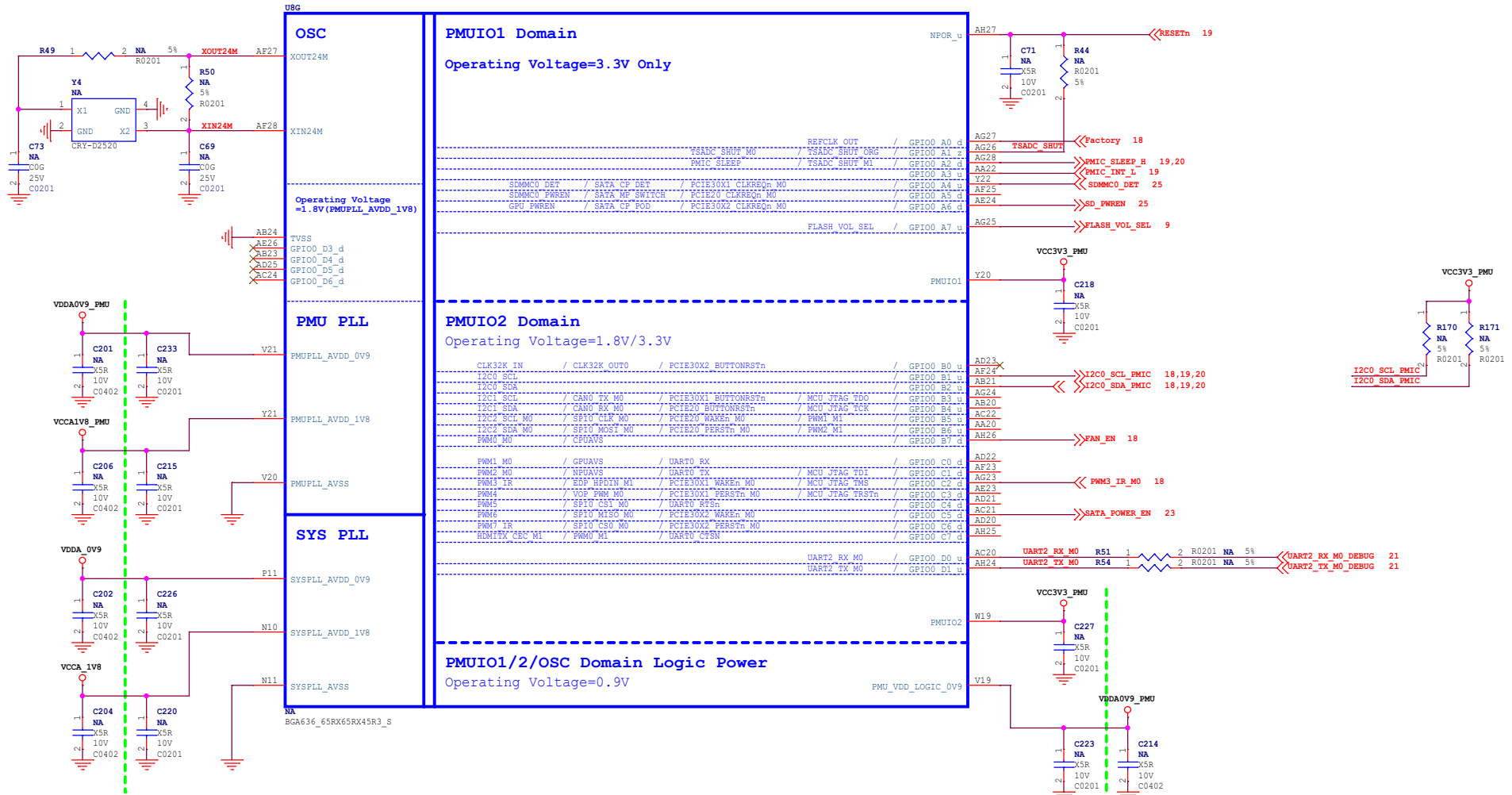
DDR3L	=1.35V	DDRRHY_VDDQ_1	H9
DDR3	=1.5V	DDRRHY_VDDQ_2	H11
DDR4	=1.2V	DDRRHY_VDDQ_3	H12
LPDDR3	=1.2V	DDRRHY_VDDQ_4	H14
LPDDR4	=1.1V	DDRRHY_VDDQ_5	J9
LPDDR4x	=1.1V	DDRRHY_VDDQ_6	L9
		DDRRHY_VDDQ_7	M9
		DDRRHY_VDDQ_8	
DDR3L	=1.35V	DDRRHY_VDDQL_1	J11
DDR3	=1.5V	DDRRHY_VDDQL_2	J12
DDR4	=1.2V	DDRRHY_VDDQL_3	J14
LPDDR3	=1.2V	DDRRHY_VDDQL_4	K10
LPDDR4	=1.1V	DDRRHY_VDDQL_5	L10
LPDDR4x	=0.6V	DDRRHY_VDDQL_6	M10



Caps should be placed under the U1000 package

HINLINK			
Project:	HNAS		Rev: <Revision>
File:	07.RK3568_DDR_PHY		
Date:	Thursday, November 30, 2023		
Designer:	<designer>		

RK3568_G (OSC/PLL/PMUIO1/2)



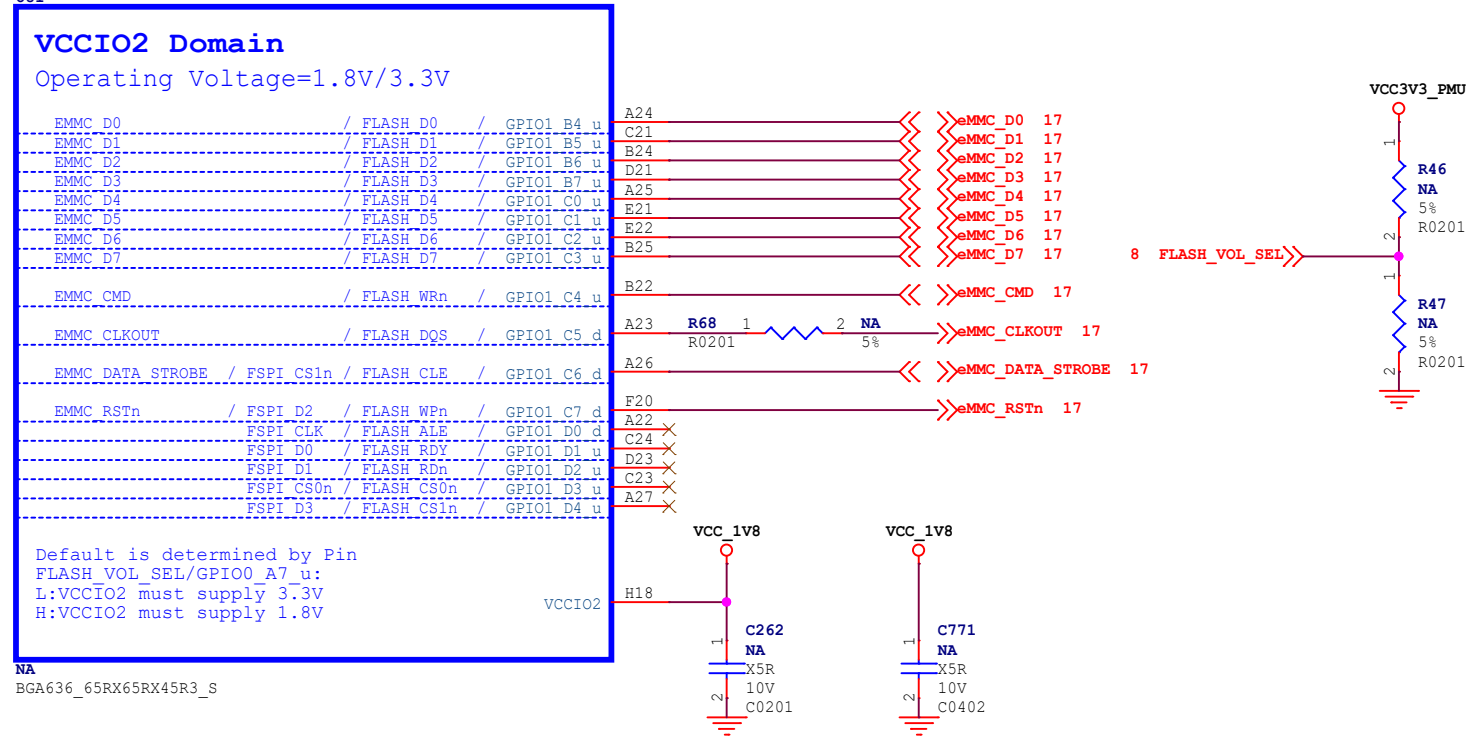
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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Project:	HNAS		Rev: <Revision>
File:	08.RK3568_OSC/PLL/PMUIO		
Date:	Thursday, November 30, 2023	Sheet:	28 of 8
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RK3568_I (VCCIO2 Domain)

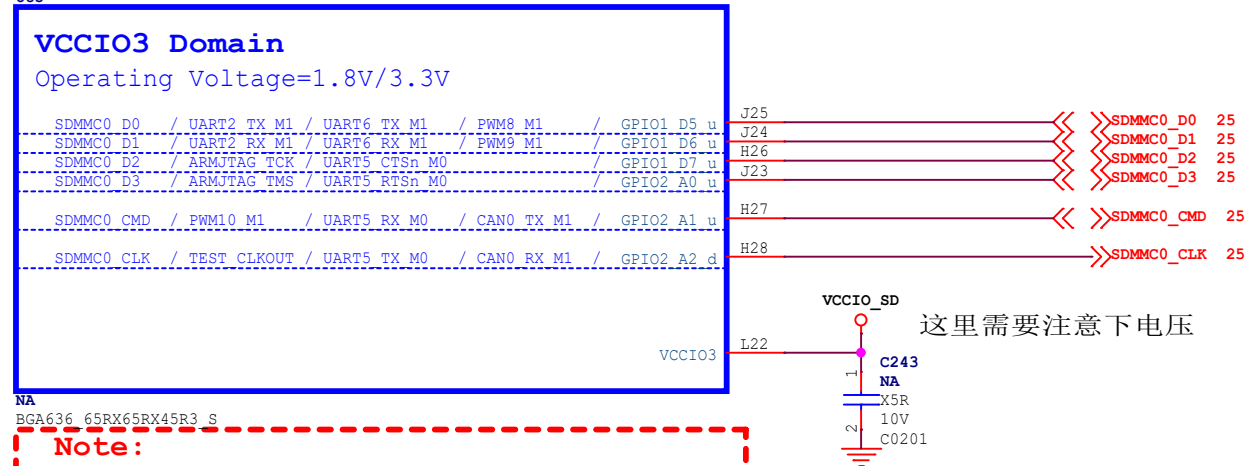
U8I



NA
BGA636_65RX65RX45R3_s

RK3568_J (VCCIO3 Domain)

U8J

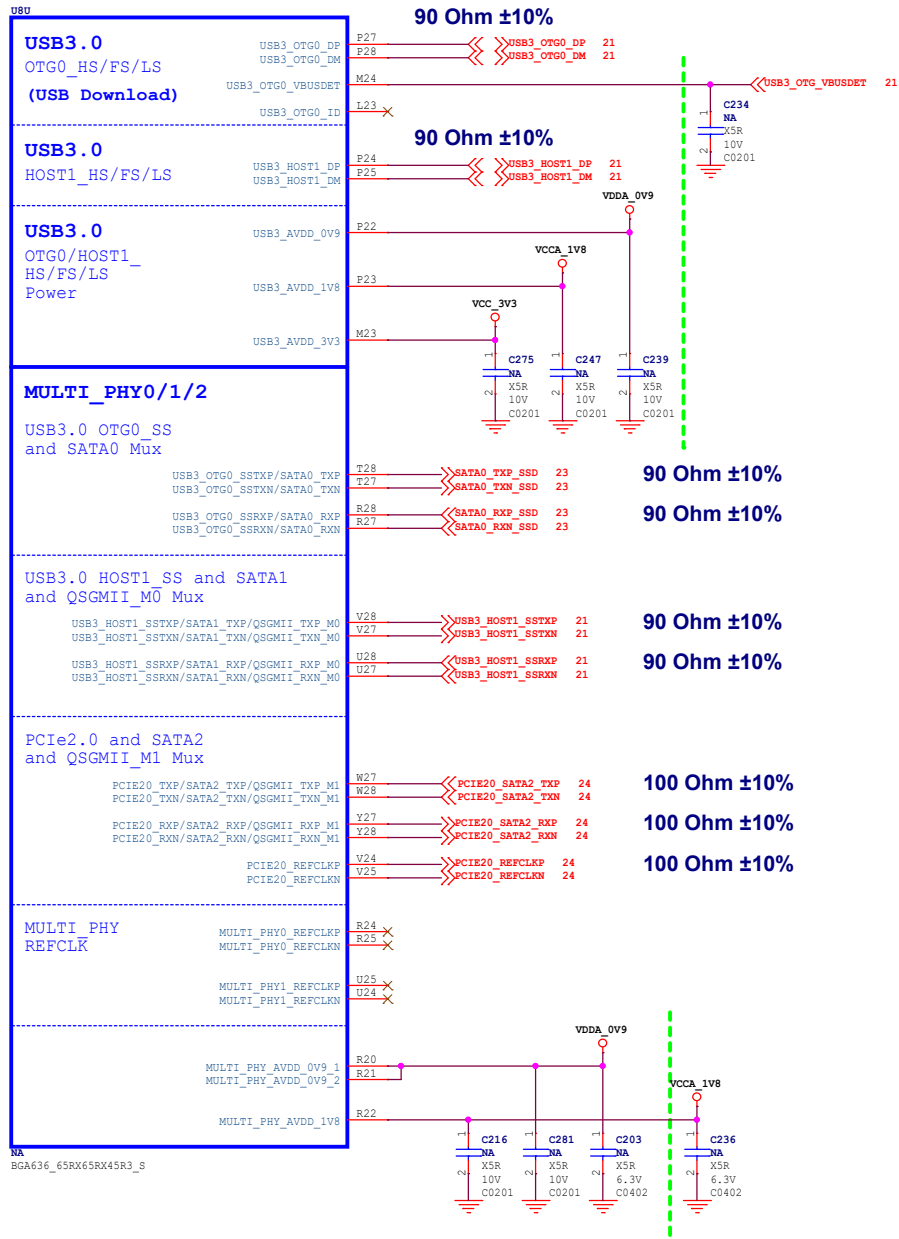


NA
BGA636_65RX65RX45R3_s

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

HINLINK			
Project:	HNAS		
File:	09.RK3568_Flash/SD Controller		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
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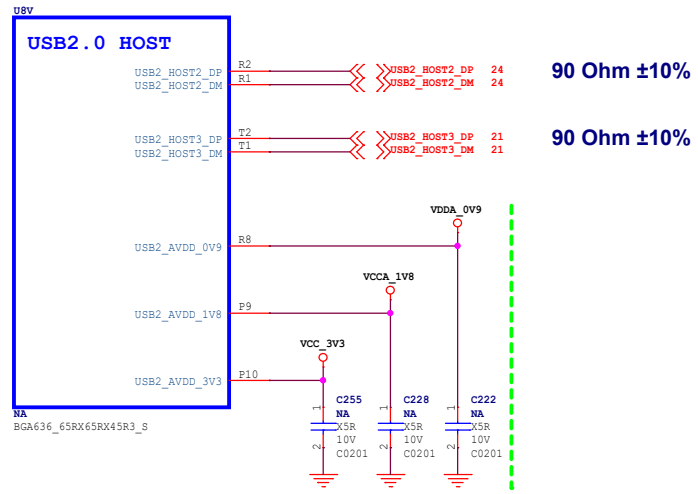
RK3568_U (USB3.0/SATA/QSGMII/PCIE2.0 x1)



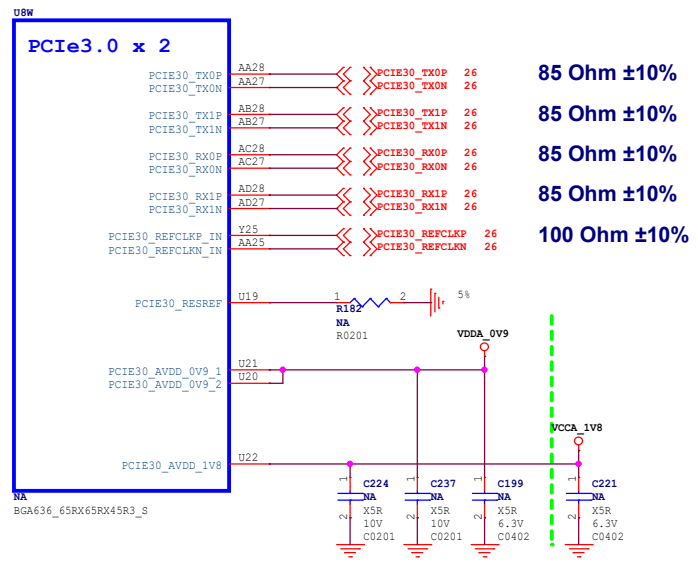
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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RK3568_V (USB2.0 HOST)

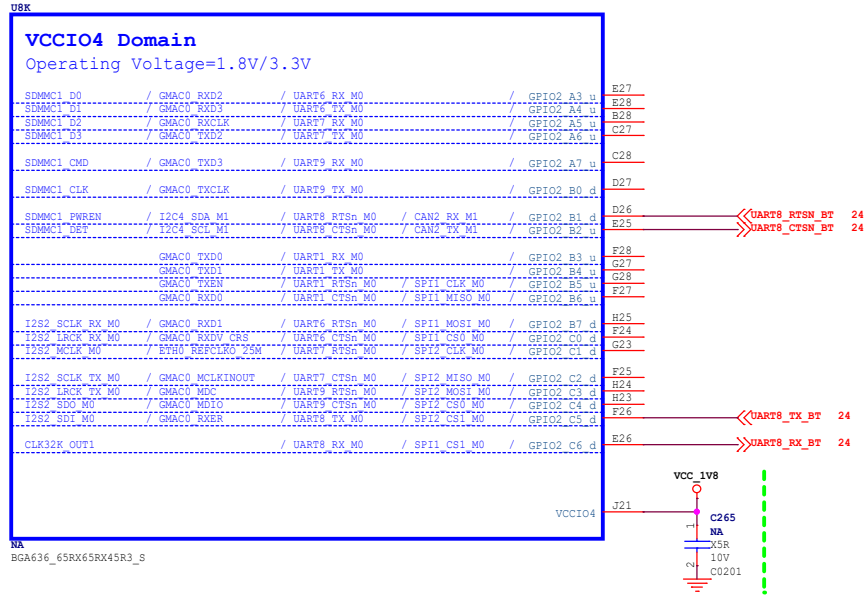


RK3568_W (PCIE3.0 x2)

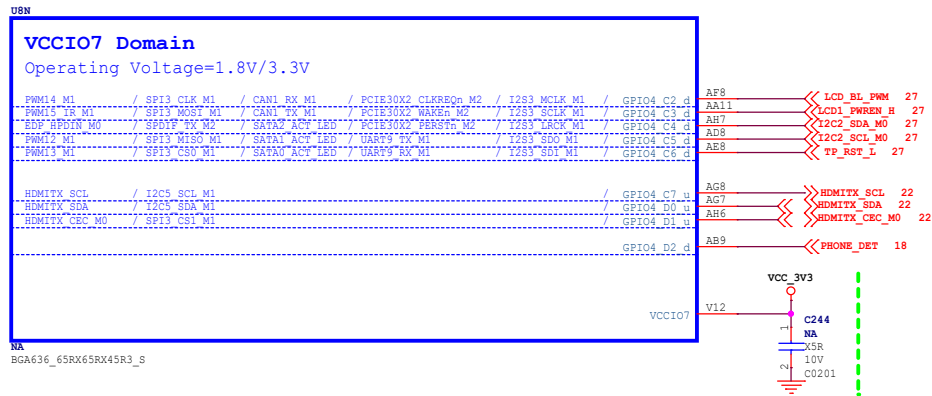


HINLINK			
Project:	HNAS		
File:	10.RK3568_USB/PCIE/SATA PHY		
Date:	Thursday, November 30, 2023		
Designer:	<designer>	Rev:	<Revision>
		Sheet:	28 of 10

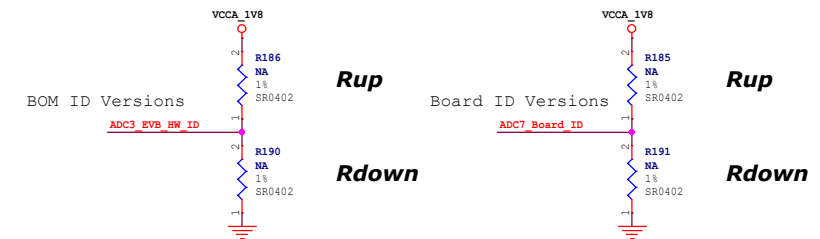
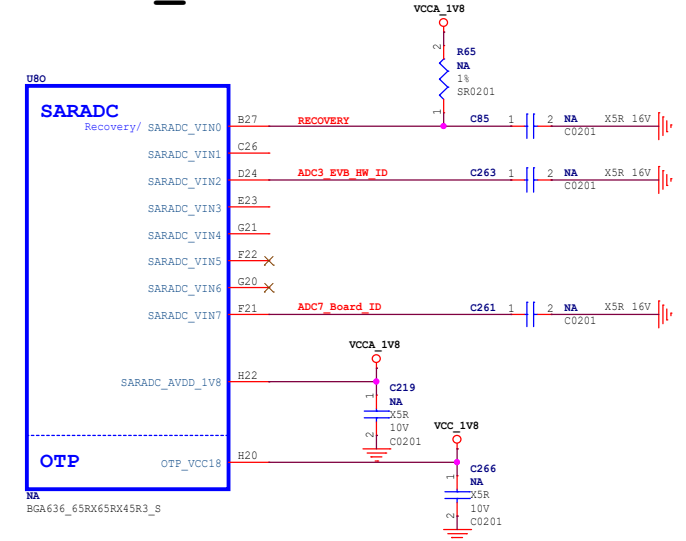
RK3568_K (VCCIO4 Domain)



RK3568_N (VCCIO7 Domain)



RK3568_O (SARADC/OTP)



BOM ID Versions TABLE 1

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	100K	2047	0.9V	V3.0
LEVEL4	100K	DNP	4096	1.8V	V4.0

Board ID Versions TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	WIFI AP6212+SATA
LEVEL2	100K	20K	682	0.3V	WIFI AP6256+SATA
LEVEL3	100K	100K	2047	0.9V	WIFI WIFI6
LEVEL4	100K	200K	4096	1.2V	WIFI NC+SATA

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

HINLINK

Project:	HNAS		
File:	11.RK3568_SARADC/GPIO		
Date:	Thursday, November 30, 2023		
Designer:	<designer>		
Rev:	<Revision>	Sheet:	28 of 11

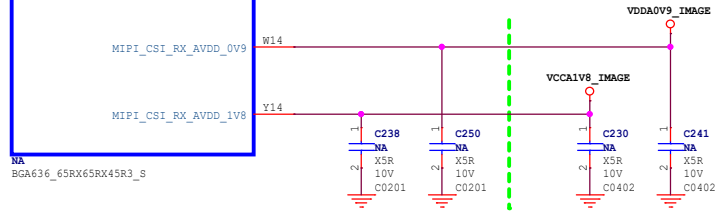
RK3568_P (MIPI_CSI_RX)

UBP

MIPI CSI RX	
MIPI_CSI_RX_D0P	AG12
MIPI_CSI_RX_D0N	AH12
MIPI_CSI_RX_D1P	AG11
MIPI_CSI_RX_D1N	AH11
MIPI_CSI_RX_D2P	AE11
MIPI_CSI_RX_D2N	AD11
MIPI_CSI_RX_D3P	AD9
MIPI_CSI_RX_D3N	AE9
MIPI_CSI_RX_CLK0P	AG10
MIPI_CSI_RX_CLK0N	AH10
MIPI_CSI_RX_CLK1P	AG9
MIPI_CSI_RX_CLK1N	AH9

MIPI_CSI_RX
100 Ohm ±10%

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

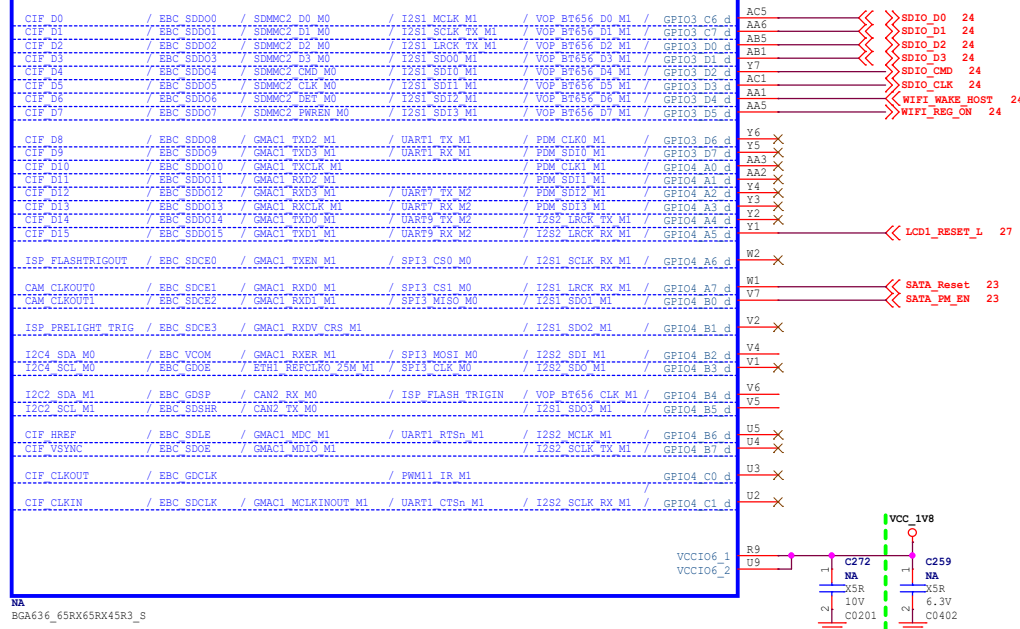


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_M (VCCIO6 Domain)

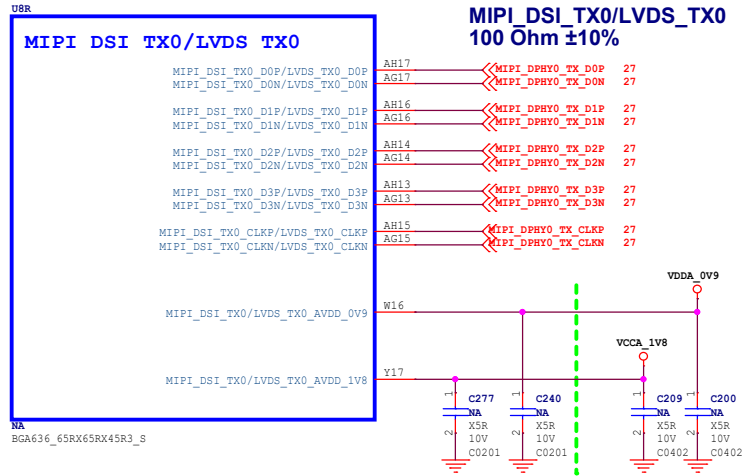
UBM

VCCIO6 Domain	
Operating Voltage=1.8V/3.3V	
CIF_D0	/ EBC SDD00 / SDMMC2 D0 M0 / I2S1 MCLK M1 / VOP BT656 D0 M1 / GPIO3 C6 d
CIF_D1	/ EBC SDD01 / SDMMC2 D1 M1 / I2S1 SCLK TX M1 / VOP BT656 D1 M1 / GPIO3 C7 d
CIF_D2	/ EBC SDD02 / SDMMC2 D2 M0 / I2S1 LCLK TX M1 / VOP BT656 D2 M1 / GPIO3 D0 d
CIF_D3	/ EBC SDD03 / SDMMC2 D3 M0 / I2S1 SD00 M1 / VOP BT656 D3 M1 / GPIO3 D1 d
CIF_D4	/ EBC SDD04 / SDMMC2 CMD M0 / I2S1 SD10 M1 / VOP BT656 D4 M1 / GPIO3 D2 d
CIF_D5	/ EBC SDD05 / SDMMC2 CLK M0 / I2S1 SD11 M1 / VOP BT656 D5 M1 / GPIO3 D3 d
CIF_D6	/ EBC SDD06 / SDMMC2 BEV M0 / I2S1 SD12 M1 / VOP BT656 D6 M1 / GPIO3 D4 d
CIF_D7	/ EBC SDD07 / SDMMC2 FWREN M0 / I2S1 SD13 M1 / VOP BT656 D7 M1 / GPIO3 D5 d
CIF_D8	/ EBC SDD08 / GMAC1 TXD2 M1 / UART1 TX M1 / PWM CLK0 M1 / GPIO3 D6 d
CIF_D9	/ EBC SDD09 / GMAC1 TXD3 M1 / UART1 RX M1 / PWM SD10 M1 / GPIO3 D7 d
CIF_D10	/ EBC SDD010 / GMAC1 TXCLK M1 / PWM CLK1 M1 / GPIO4 A0 d
CIF_D11	/ EBC SDD011 / GMAC1 RXD2 M1 / DARGEN_TX M2 / PWM SD11 M1 / GPIO4 A1 d
CIF_D12	/ EBC SDD012 / GMAC1 RXD3 M1 / DARGEN_RX M2 / PWM SD12 M1 / GPIO4 A2 d
CIF_D13	/ EBC SDD013 / GMAC1 RXD4 M1 / DARGEN_TX M2 / PWM SD13 M1 / GPIO4 A3 d
CIF_D14	/ EBC SDD014 / GMAC1 RXD0 M1 / DARGEN_RX M2 / VOP BT656 TX M1 / GPIO4 A4 d
CIF_D15	/ EBC SDD015 / GMAC1 RXD1 M1 / DARGEN_RX M2 / VOP BT656 TX M1 / GPIO4 A5 d
ISP_FLASHTRIGOUT	/ EBC SDC00 / GMAC1 TXEN M1 / SPI3 CS0 M0 / I2S1 SCLK RX M1 / GPIO4 A6 d
CAN_CLKOUT0	/ EBC SDC01 / GMAC1 RXD0 M1 / SPI3 CS1 M0 / I2S1 LRCK RX M1 / GPIO4 A7 d
CAN_CLKOUT1	/ EBC SDC02 / GMAC1 RXD1 M1 / SPI3 MISO M0 / I2S1 SD01 M1 / GPIO4 B0 d
ISP_PRELIGHT_TRIG	/ EBC SDC03 / GMAC1 RXDV CRS M1 / I2S1 SD02 M1 / GPIO4 B1 d
I2C4_SDA M0	/ EBC VCOM / GMAC1 RXER M1 / SPI3 MOSI M0 / I2S2 SD1 M1 / GPIO4 B2 d
I2C4_SCL M0	/ EBC SDC04 / EPH1 REFCLK0 TX M1 / SPI3 CS2 M0 / I2S2 SDO M1 / GPIO4 B3 d
I2C2_SDA M1	/ EBC GDS0 / CAN2 RX M0 / ISP_FLASH_TRIGIN / VOP BT656 CLK M1 / GPIO4 B4 d
I2C2_SCL M1	/ EBC SDC05 / CAN2 TX M0 / I2S1 SD03 M1 / GPIO4 B5 d
CIF_HREF	/ EBC SDLE / GMAC1 MDC M1 / UART1 RTS M1 / I2S2 MCLK M1 / GPIO4 B6 d
CIF_VSYNC	/ EBC SDC06 / GMAC1 MDC M1 / I2S2 SCLK TX M1 / GPIO4 B7 d
CIF_CLKOUT	/ EBC GDC0 / GMAC1 MDC M1 / PWM1 IR M1 / GPIO4 C0 d
CIF_CLKIN	/ EBC SDC07 / GMAC1 MCLKINOUT M1 / UART1 CTS M1 / I2S2 SCLK RX M1 / GPIO4 C1 d

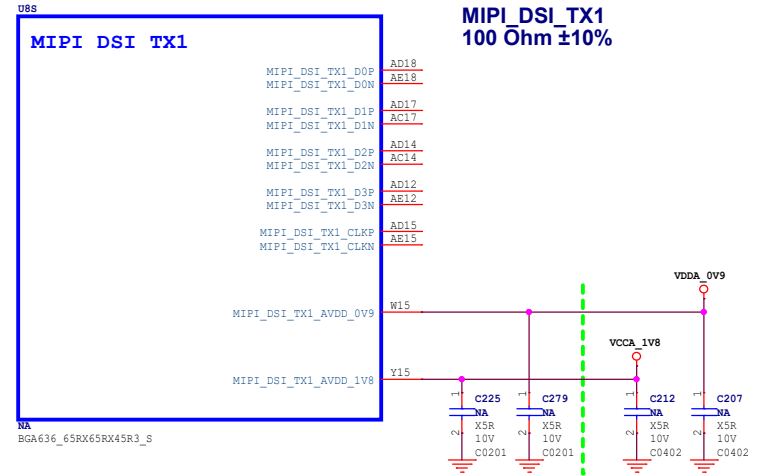


HINLINK			
Project:	HNAS		
File:	12.RK3568_VI Interface		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 12

RK3568_R (MIPI_DSI_TX0/LVDS_TX0)

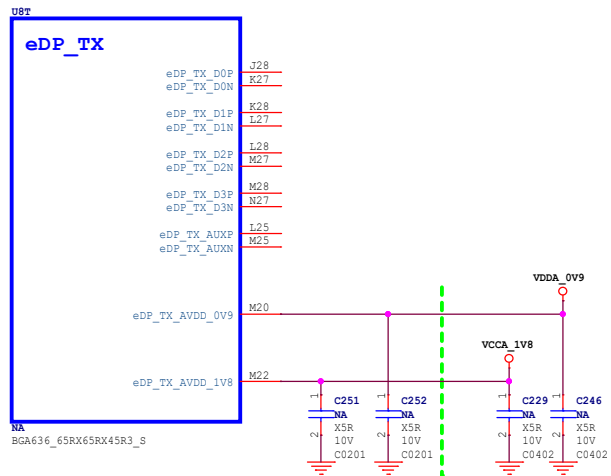


RK3568_S (MIPI_DSI_TX1)



RK3568_T (eDP TX)

eDP TX 100 Ohm ±10%

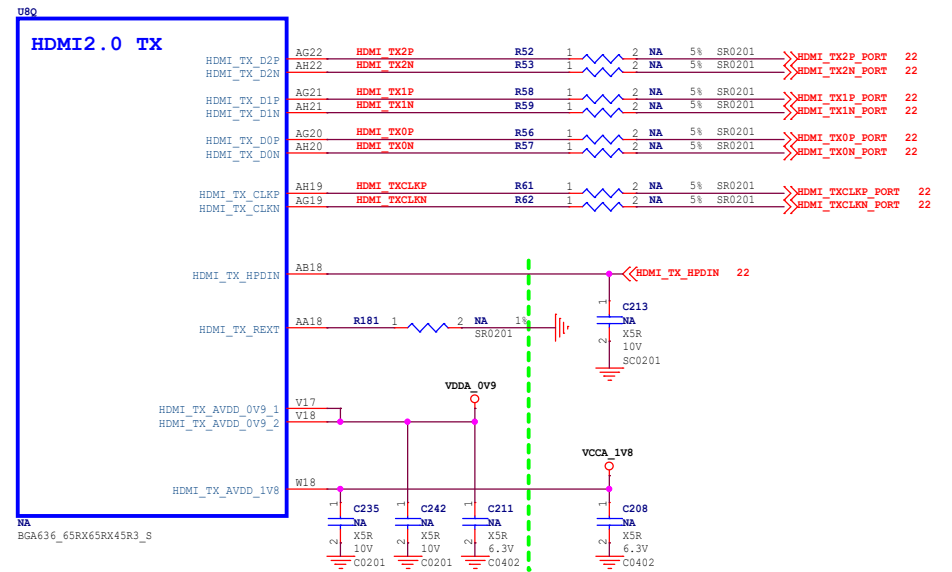


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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RK3568_Q (HDMI2.0 TX)

HDMI TMDs trace 100 Ohm ±10%



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Project:	HNAS	Rev:	<Revision>
File:	13.RK3568_VO Interface_1	Sheet:	28 of 13
Date:	Thursday, November 30, 2023	Designer:	<designer>

RK3568_L (VCCIO5 Domain)

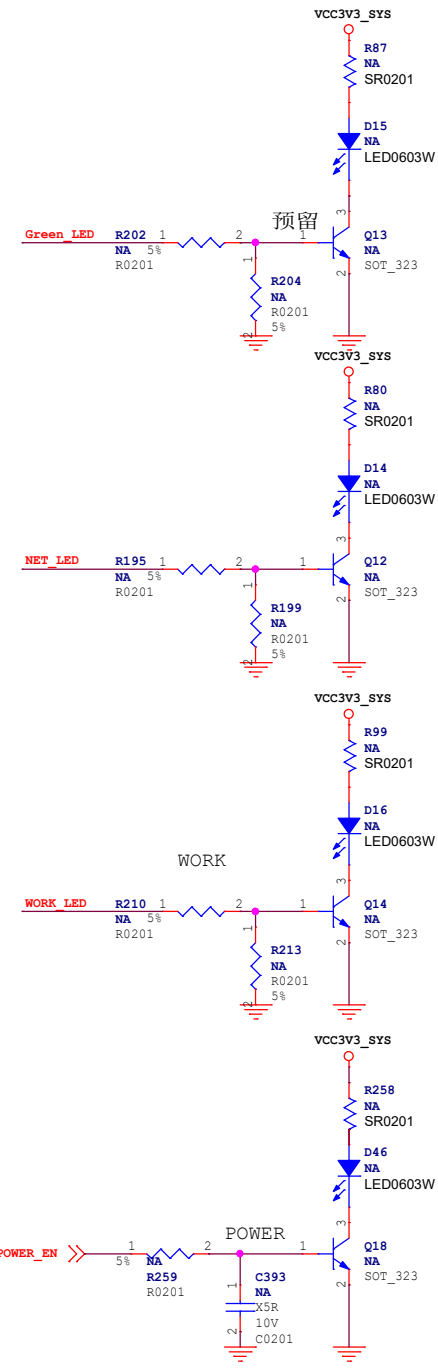
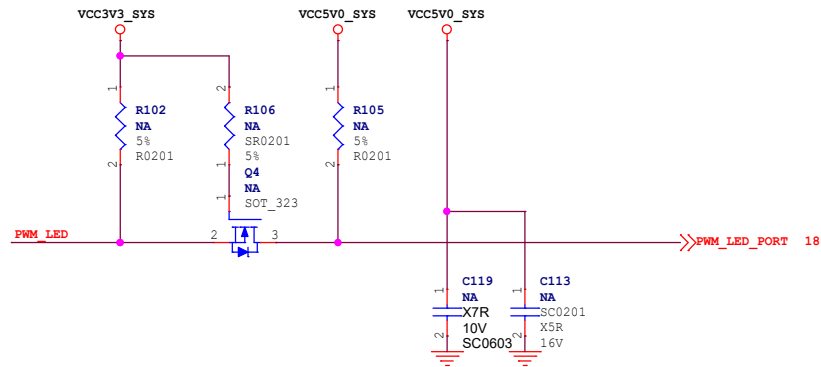
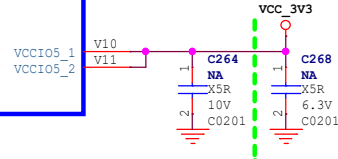
U8L

VCCIO5 Domain


Operating Voltage=1.8V/3.3V

LCDC D0 / VOP BT656 D0 M0 / SPI0 MISO M1 / PCIE20 CLKREOn M1 / I2S1 MCLK M2 / GPIO2 D0 d	AG6	>>>25GLAN_ResetA 26
LCDC D1 / VOP BT656 D1 M0 / SPI0 MOSI M1 / PCIE20 WAKEn M1 / I2S1 SCLK TX M2 / GPIO2 D1 d	AD7	X
LCDC D2 / VOP BT656 D2 M0 / SPI0 CS0 M1 / PCIE30X1 CLKREOn M1 / I2S1 LRCK TX M2 / GPIO2 D2 d	AC8	X
LCDC D3 / VOP BT656 D3 M0 / SPI0 CLK M1 / PCIE30X1 WAKEn M1 / I2S1 SDIO M2 / GPIO2 D3 d	AC7	X
LCDC D4 / VOP BT656 D4 M0 / SPI2 CS1 M1 / PCIE30X2 CLKREOn M1 / I2S1 SDI1 M2 / GPIO2 D4 d	AF5	>>>PCIE30X2 CLKREOn M1 3V3 24
LCDC D5 / VOP BT656 D5 M0 / SPI2 CS0 M1 / PCIE30X2 WAKEn M1 / I2S1 SDI2 M2 / GPIO2 D5 d	AF6	>>>PCIE30X2 WAKEn M1 3V3 24
LCDC D6 / VOP BT656 D6 M0 / SPI2 MOSI M1 / PCIE30X2 PERSTn M1 / I2S1 SDI3 M2 / GPIO2 D6 d	AD6	>>>PCIE30X2 PERSTn M1 3V3 24
LCDC D7 / VOP BT656 D7 M0 / SPI2 MISO M1 / UART8 TX M1 / I2S1 SDO0 M2 / GPIO2 D7 d	AH5	X
LCDC CLK / VOP BT656 CLK M0 / SPI2 CLK M1 / UART8 RX M1 / I2S1 SDO1 M2 / GPIO3 A0 d	AH4	>>>BT_REG_ON 24
LCDC D8 / VOP BT1120 D0 / SPI1 CS0 M1 / PCIE30X1 PERSTn M1 / SDMMC2 D0 M1 / GPIO3 A1 d	AB8	>>>BT_WAKE_HOST 24
LCDC D9 / VOP BT1120 D1 / GMAC1 TXD3 M0 / I2S3 MCLK M0 / SDMMC2 D1 M1 / GPIO3 A2 d	AE5	>>>HOST_WAKE_BT 24
LCDC D10 / VOP BT1120 D2 / GMAC1 TXD3 M0 / I2S3 SCLK M0 / SDMMC2 D2 M1 / GPIO3 A3 d	AG4	X
LCDC D11 / VOP BT1120 D3 / GMAC1 RXD2 M0 / I2S3 LRCK M0 / SDMMC2 D3 M1 / GPIO3 A4 d	AF4	X
LCDC D12 / VOP BT1120 D4 / GMAC1 RXD3 M0 / I2S3 SDO M0 / SDMMC2 CMD M1 / GPIO3 A5 d	AH3	Green LED >>>25GLAN_ResetB 26
LCDC D13 / VOP BT1120 D5 / GMAC1 TXCLK M0 / I2S3 SDI M0 / SDMMC2 CLK M1 / GPIO3 A6 d	AG3	X
LCDC D14 / VOP BT1120 D6 / GMAC1 RXCLK M0 / I2S3 SDO M0 / SDMMC2 DET M1 / GPIO3 A7 d	AH2	NET LED
LCDC D15 / VOP BT1120 D7 / ETH1 REFCLK0 25M M0 / SDMMC2 PWREN M1 / GPIO3 B0 d	AG2	WORK LED
LCDC D16 / VOP BT1120 D7 / GMAC1 RXD0 M0 / UART4 RX M1 / PWM8 M0 / GPIO3 B1 d	AG1	X
LCDC D17 / VOP BT1120 D8 / GMAC1 RXD1 M0 / UART4 TX M1 / PWM9 M0 / GPIO3 B2 d	AF2	>>>SATA3_LED 23
LCDC D18 / VOP BT1120 D9 / GMAC1 RXDV CRS M0 / I2C5 SCL M0 / PDM SDI0 M2 / GPIO3 B3 d	AF1	>>>SATA2_LED 23
LCDC D19 / VOP BT1120 D10 / GMAC1 RXER M0 / I2C5 SDA M0 / PDM SDI1 M2 / GPIO3 B4 d	AE1	>>>I2C5_SCL_3V3 18
LCDC D20 / VOP BT1120 D11 / GMAC1 TXD0 M0 / I2C3 SCL M1 / PWM10 M0 / GPIO3 B5 d	AE2	>>>I2C5_SDA_3V3 18
LCDC D21 / VOP BT1120 D12 / GMAC1 TXD1 M0 / I2C3 SDA M1 / PWM11 IR M0 / GPIO3 B6 d	AE3	>>>SATA1_LED 23
LCDC D22 / PWM12 M0 / GMAC1 TXEN M0 / UART3 TX M1 / PDM SDI2 M2 / GPIO3 B7 d	AD4	>>>SATA0_LED 23
LCDC D23 / PWM13 M0 / GMAC1 MCLKINOUT M0 / UART3 RX M1 / PDM SDI3 M2 / GPIO3 C0 d	AD2	>>>EPI_INT_L 27 >>>KEY 24
LCDC HSYNC / VOP BT1120 D13 / SPI1 MOSI M1 / PCIE20 PERSTn M1 / I2S1 SDO2 M2 / GPIO3 C1 d	AD1	>>>Reset_Zigbee 24
LCDC VSYNC / VOP BT1120 D14 / SPI1 MISO M1 / UART5 TX M1 / I2S1 SDO3 M2 / GPIO3 C2 d	AA7	>>>UART5_TX_Zigbee 24
LCDC DEN / VOP BT1120 D15 / SPI1 CLK M1 / UART5 RX M1 / I2S1 SCLK RX M2 / GPIO3 C3 d	AC4	>>>UART5_RX_Zigbee 24
PWM14 M0 / VOP_PWM M1 / GMAC1 MDC M0 / UART7 TX M1 / PDM CLK1 M2 / GPIO3 C4 d	AC3	PWM LED
PWM15 IR M0 / SPDIF TX M1 / GMAC1 MDIO M0 / UART7 RX M1 / I2S1 LRCK RX M2 / GPIO3 C5 d	AC2	X

NA BGA636_65RX65RX45R3_S



HINLINK

Project:	HNAS	
File:	14.RK3568_VO Interface_2	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 14

RK3568_H (VCCIO1 Domain)

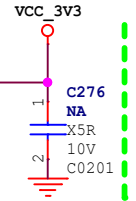
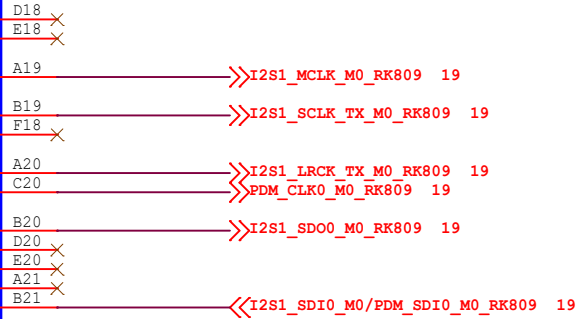
U8H

VCCIO1 Domain


Operating Voltage=1.8V/3.3V

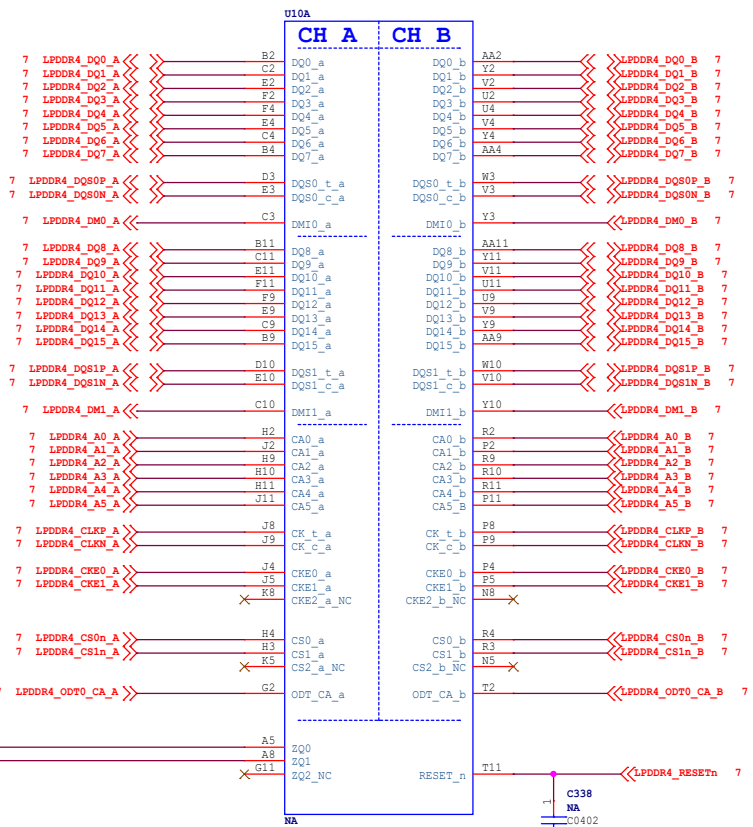
I2C3 SDA M0	/	UART3 RX M0	/	CAN1 RX M0	/	AUDIOPWM LOUT P	/	ACODEC ADC DATA	/	GPIO1 A0 u
I2C3 SCL M0	/	UART3 TX M0	/	CAN1 TX M0	/	AUDIOPWM LOUT N	/	ACODEC ADC CLK	/	GPIO1 A1 u
I2S1 MCLK M0	/	UART3 RTSn M0	/	SCR CLK	/	PCIE30X1 PERSTn M2	/		/	GPIO1 A2 d
I2S1 SCLK TX M0	/	UART3 CTSn M0	/	SCR IO	/	PCIE30X1 WAKEn M2	/	ACODEC DAC CLK	/	GPIO1 A3 d
I2S1 SCLK RX M0	/	UART4 RX M0	/	PDM CLK1 M0	/	SPDIF TX M0	/		/	GPIO1 A4 d
I2S1 LRCK TX M0	/	UART4 RTSn M0	/	SCR RST	/	PCIE30X1 CLKREOn M2	/	ACODEC DAC SYNC	/	GPIO1 A5 d
I2S1 LRCK RX M0	/	UART4 TX M0	/	PDM CLK0 M0	/	AUDIOPWM ROUT P	/		/	GPIO1 A6 d
I2S1 SDO0 M0	/	UART4 CTSn M0	/	SCR DET	/	AUDIOPWM ROUT N	/	ACODEC DAC DATAL	/	GPIO1 A7 d
I2S1 SDO1 M0	/	I2S1 SDI3 M0	/	PDM SDI3 M0	/	PCIE20 CLKREOn M2	/	ACODEC DAC DATAR	/	GPIO1 B0 d
I2S1 SDO2 M0	/	I2S1 SDI2 M0	/	PDM SDI2 M0	/	PCIE20 WAKEn M2	/	ACODEC ADC SYNC	/	GPIO1 B1 d
I2S1 SDO3 M0	/	I2S1 SDI1 M0	/	PDM SDI1 M0	/	PCIE20 PERSTn M2	/		/	GPIO1 B2 d
		I2S1 SDI0 M0	/	PDM SDI0 M0	/		/		/	GPIO1 B3 d

VCCIO1

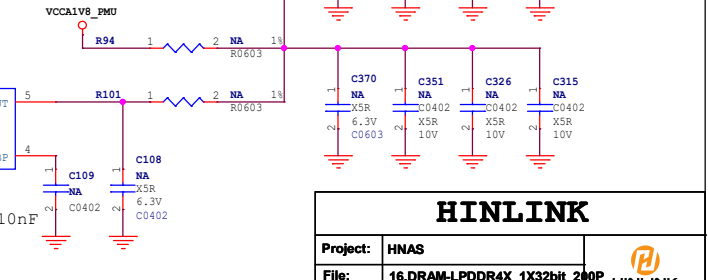
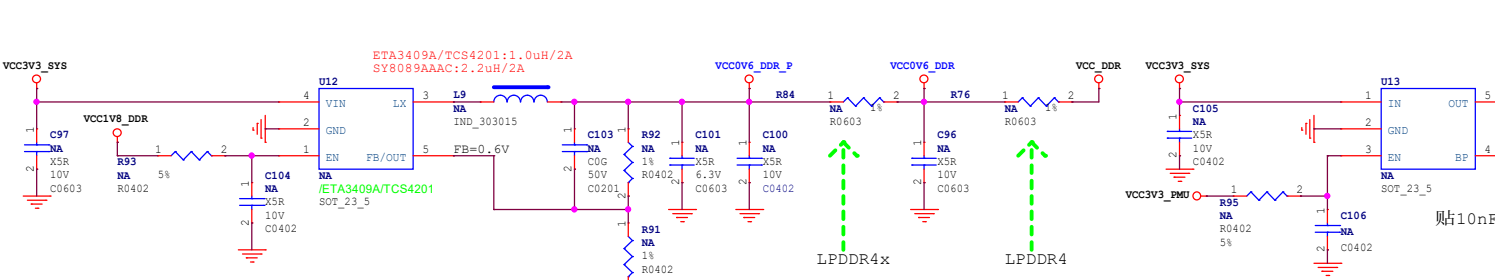
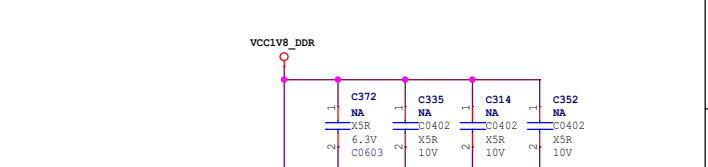
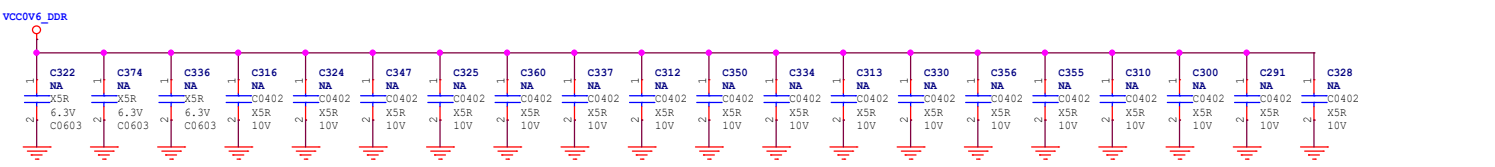
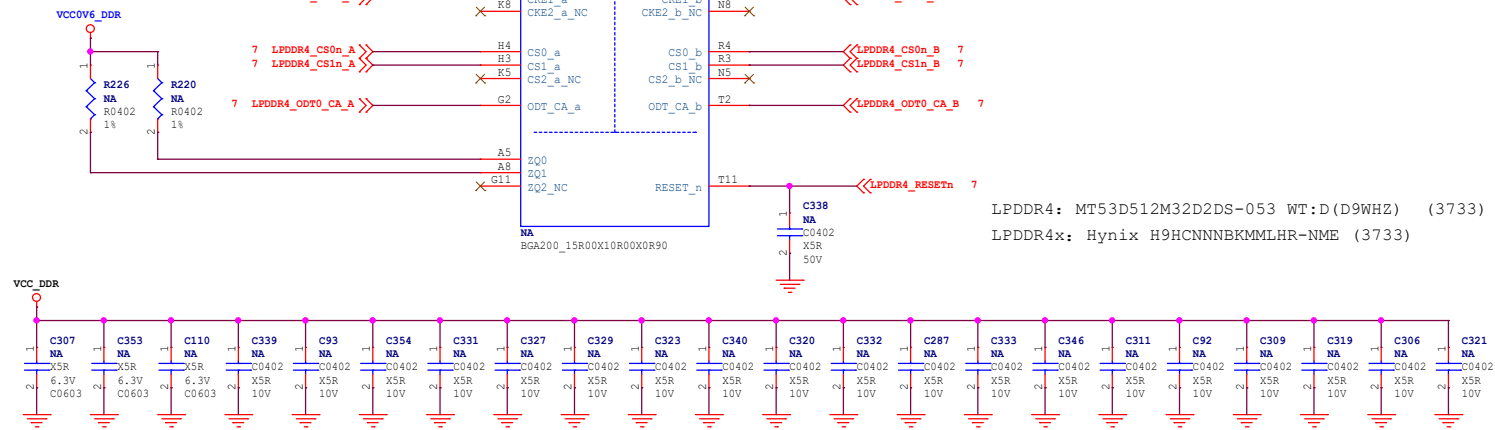
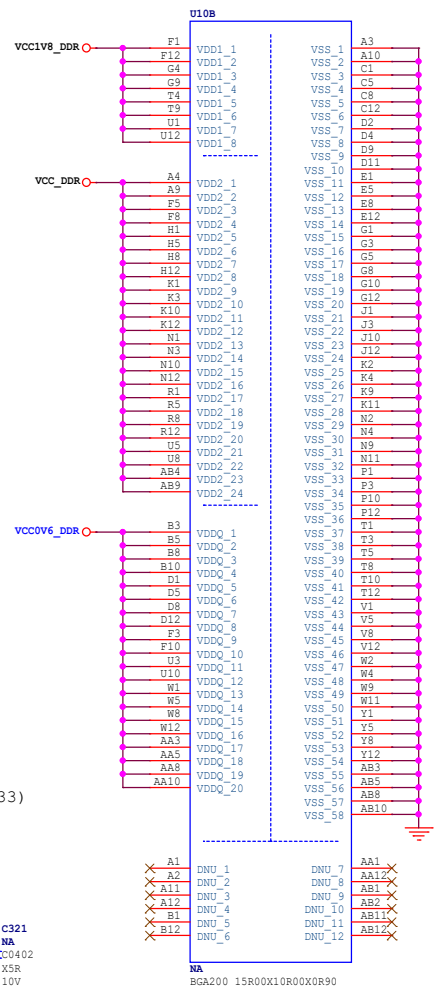


NA
BGA636_65RX65RX45R3_S

HINLINK			
Project:	HNAS	 HINLINK	
File:	15.RK3568_Audio Interface		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 15



LPDDR4: MT53D512M32D2DS-053 WT:D(D9WHZ) (3733)
 LPDDR4x: Hynix H9HCNNNBKMLHR-NME (3733)



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HINLINK	
Project: HNAS	Rev: <Revision>
File: 16.DRAM-LPDDR4X_1X32bit_240P	Sheet: 28 of 16
Date: Thursday, November 30, 2023	Designer: <designer>

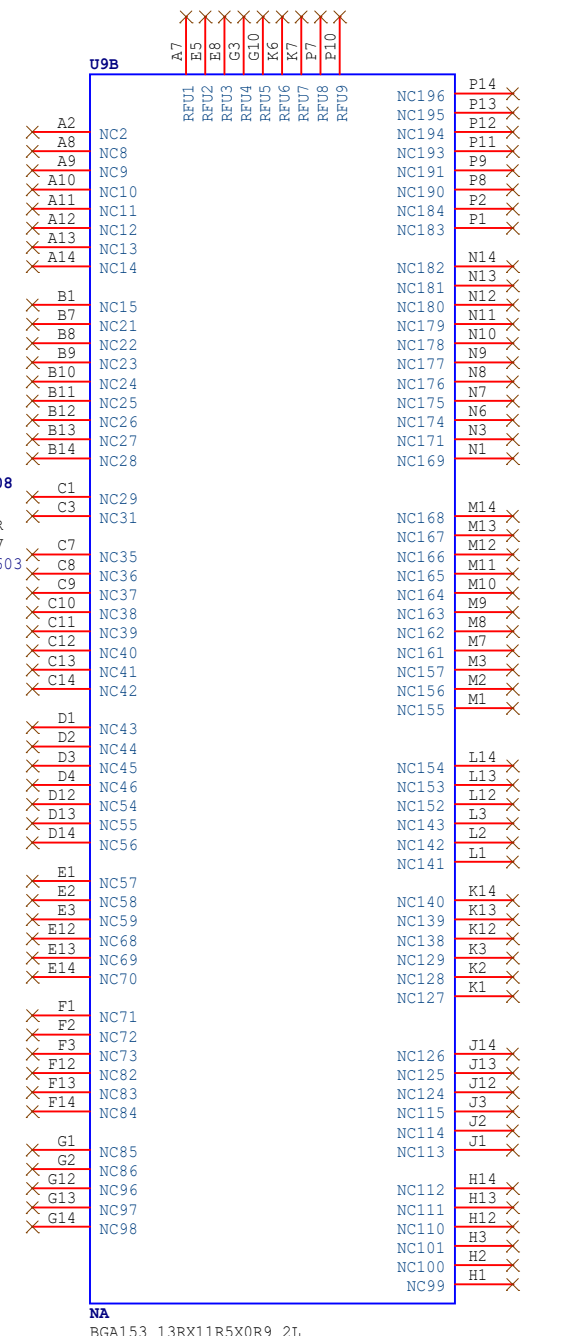
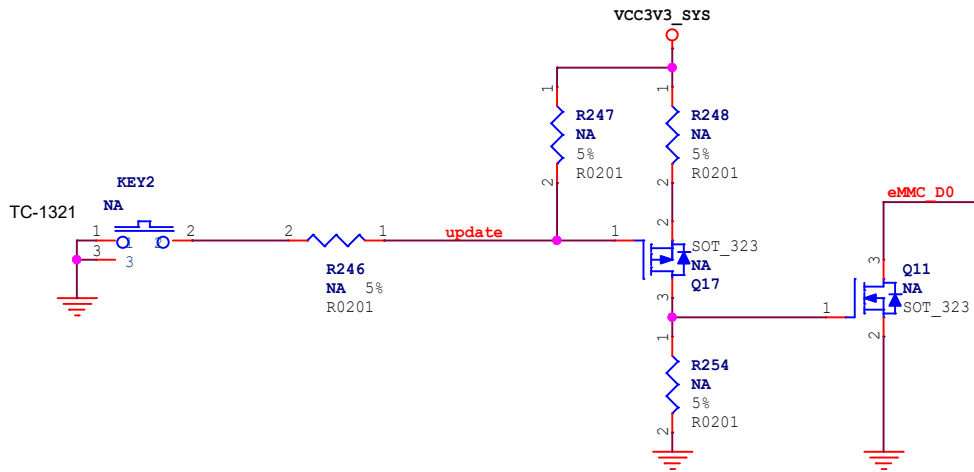
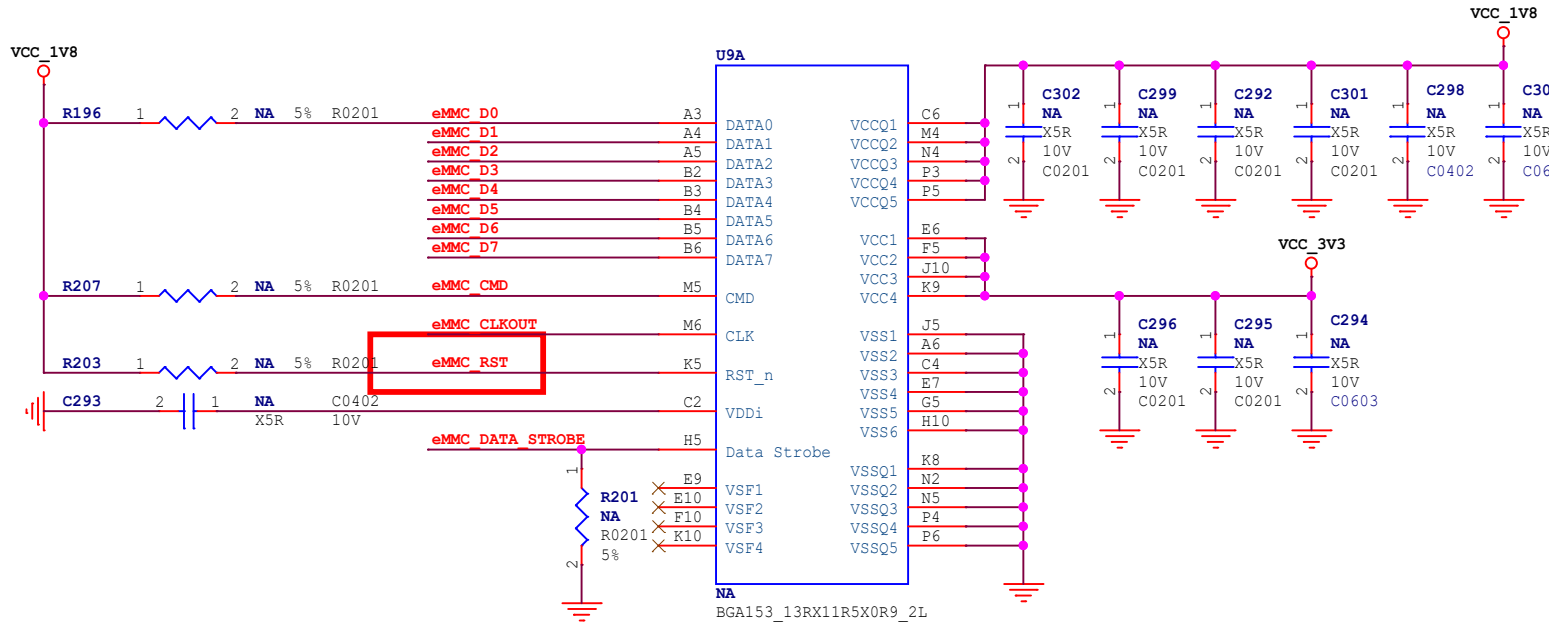
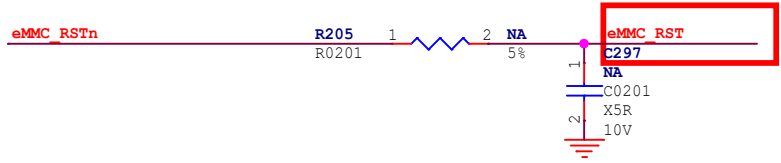
>>eMMC_D0 9
 >>eMMC_D1 9
 >>eMMC_D2 9
 >>eMMC_D3 9
 >>eMMC_D4 9
 >>eMMC_D5 9
 >>eMMC_D6 9
 >>eMMC_D7 9

 >>eMMC_CMD 9

 >>eMMC_CLKOUT 9

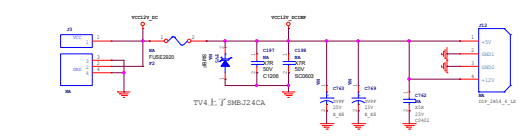
 >>eMMC_DATA_STROBE 9

 >>eMMC_RSTn 9

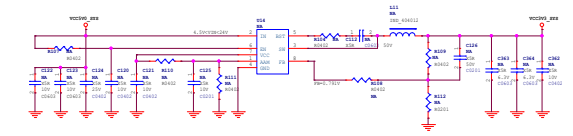
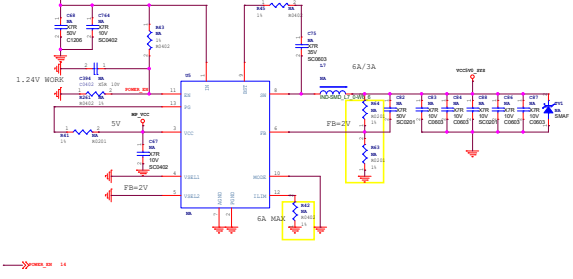


HINLINK		
Project:	HNAS	
File:	17.Flash-eMMC Flash	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 17

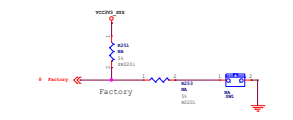
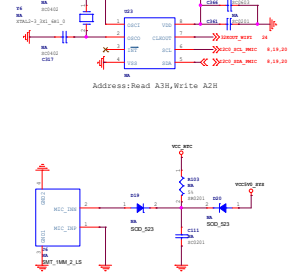
12-24V/3A DCIN



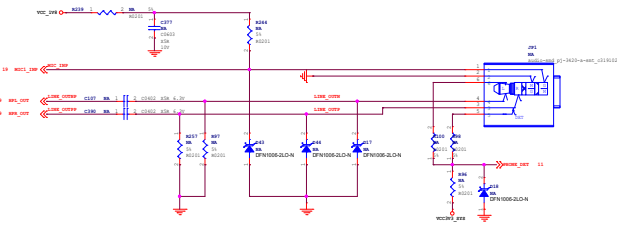
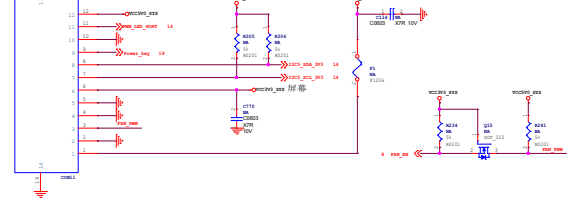
VCC5V0_SYS



RTC IC



POWER_KEY

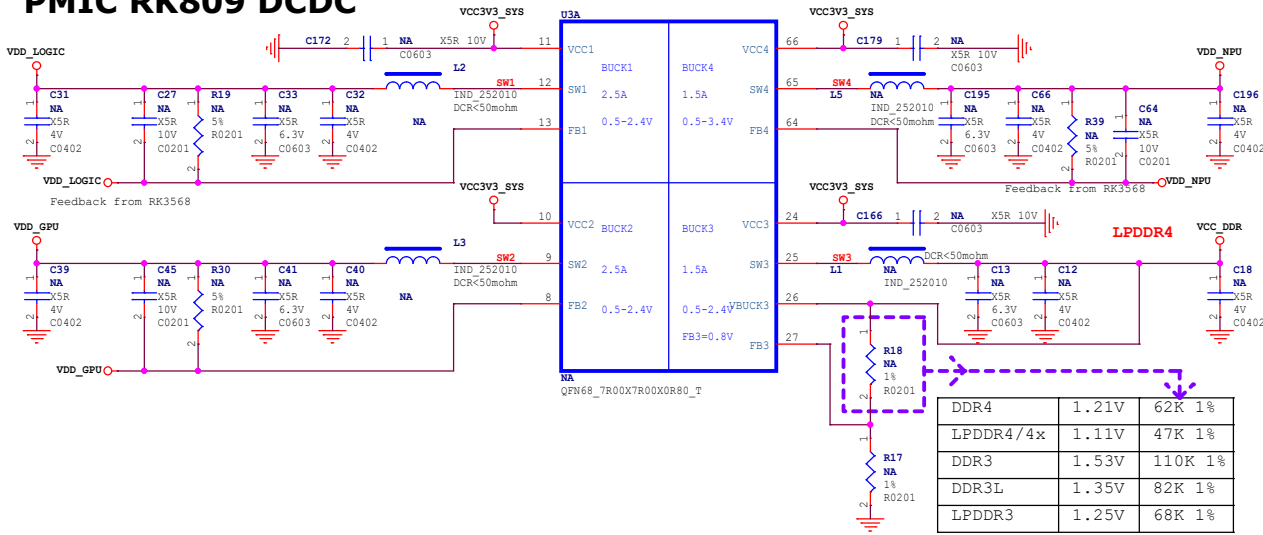


IR Receiver

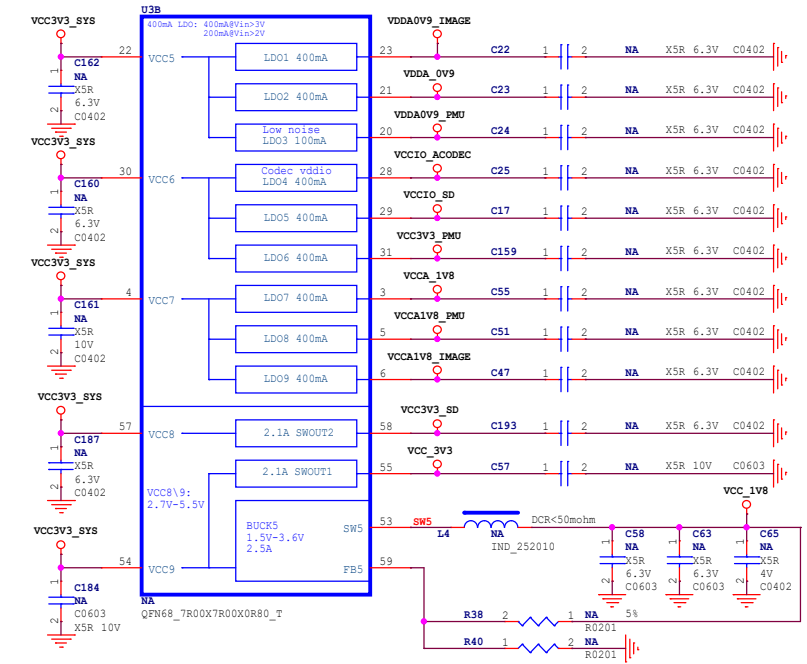


I2CO_SCL_PMIC 8,18,20
 I2CO_SDA_PMIC 8,18,20
 PMIC_INT_L 8
 PMIC_SLEEP_H 8,20
 RESETh 8,19

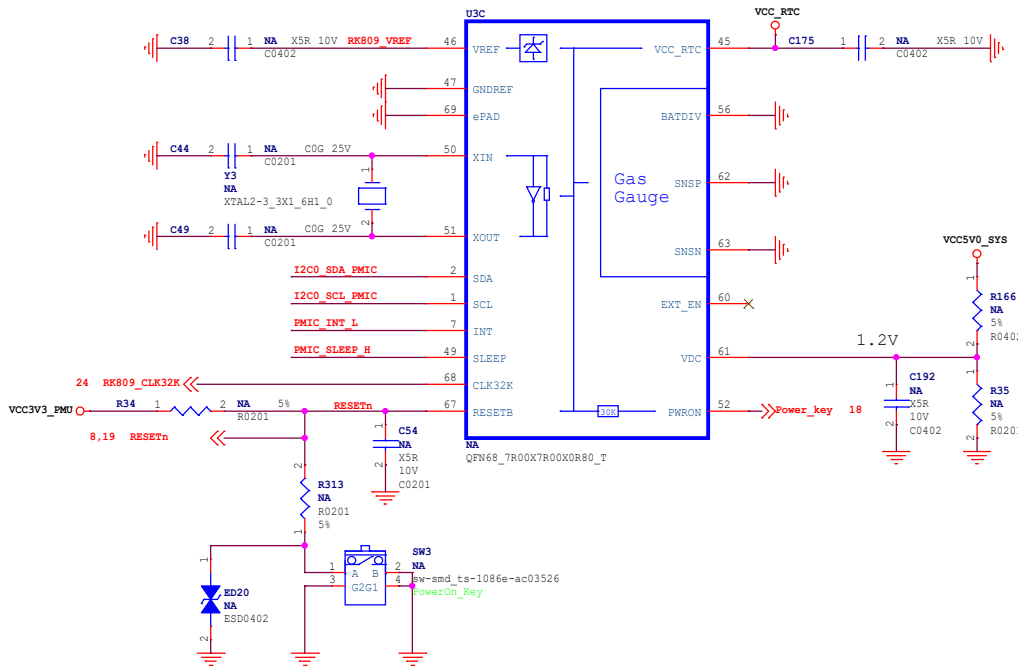
PMIC RK809 DCDC



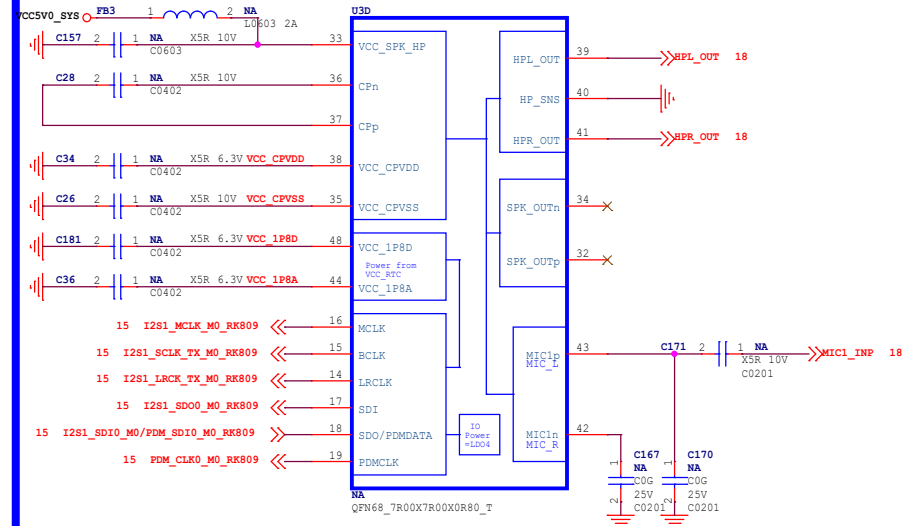
PMIC RK809 LDO



PMIC RK809 Management



PMIC RK809 CODEC

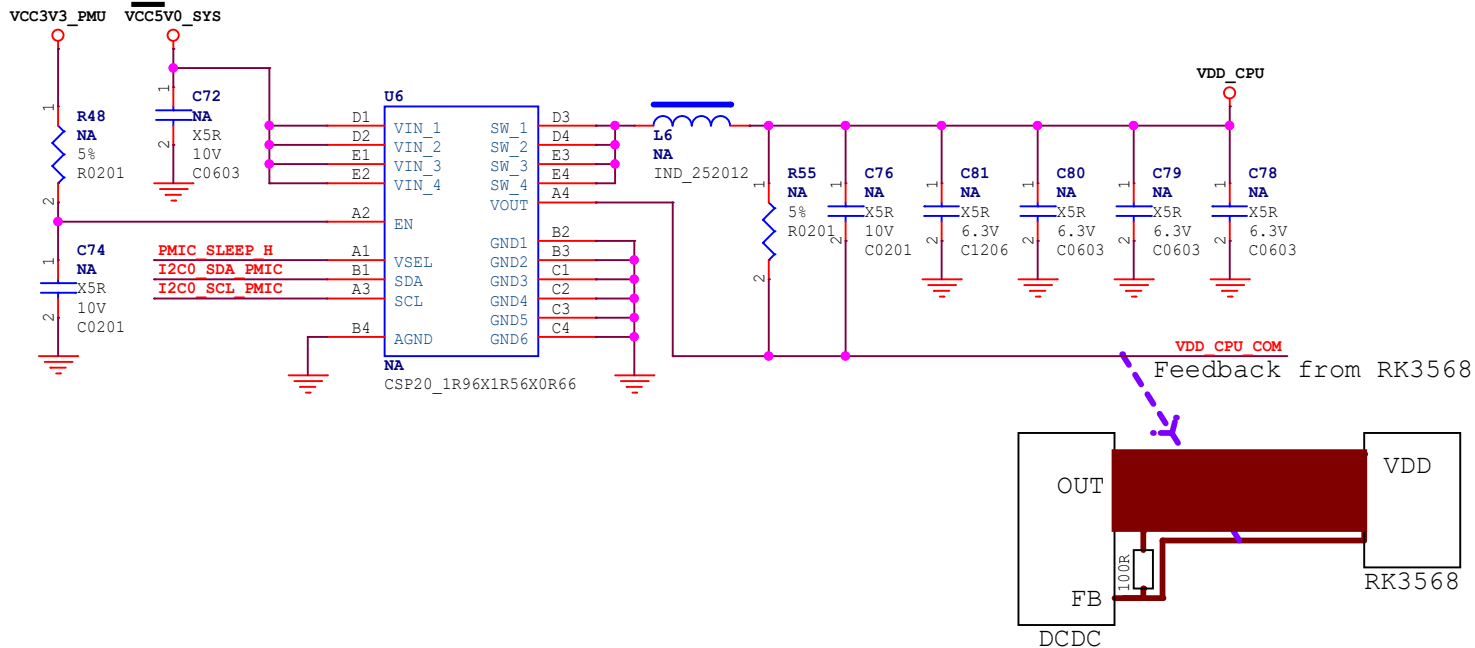


HINLINK

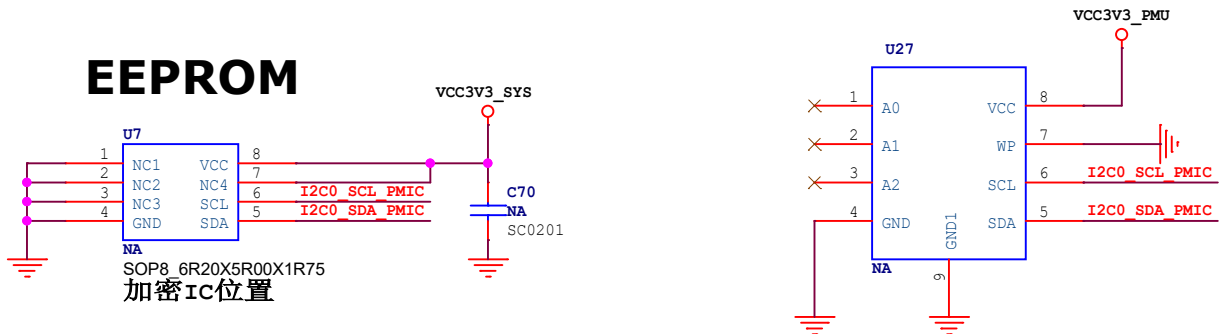
Project:	HNAS		
File:	19.Power_PMIC		
Date:	Thursday, November 30, 2023		
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>>PMIC_SLEEP_H 8,19
 <<VDD_CPU_COM 6
 >>I2C0_SCL_PMIC 8,18,19
 <<I2C0_SDA_PMIC 8,18,19

VDD_CPU



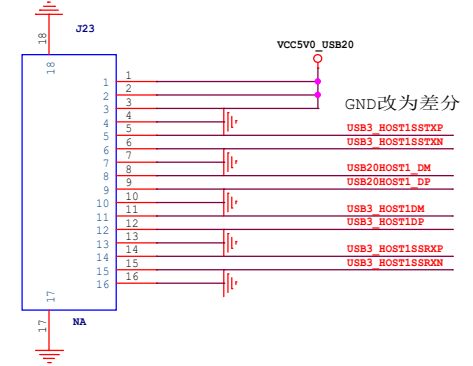
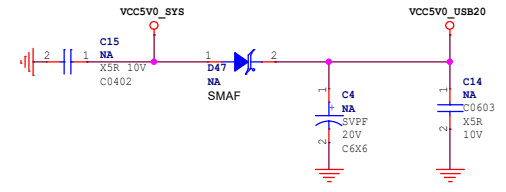
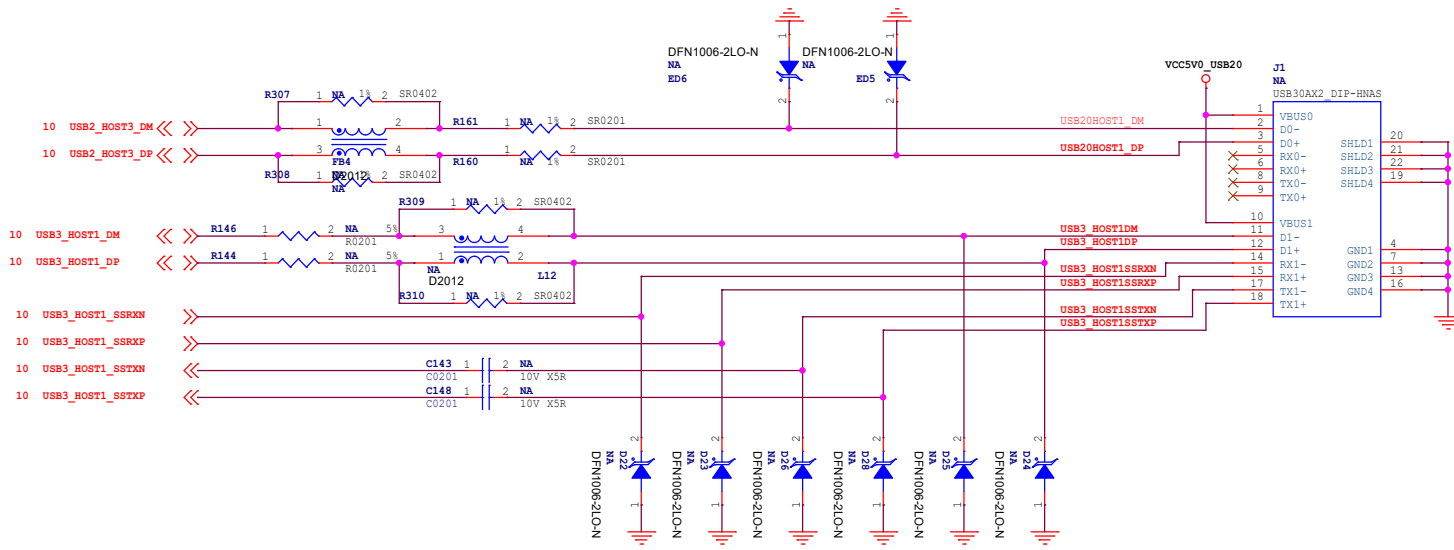
EEPROM



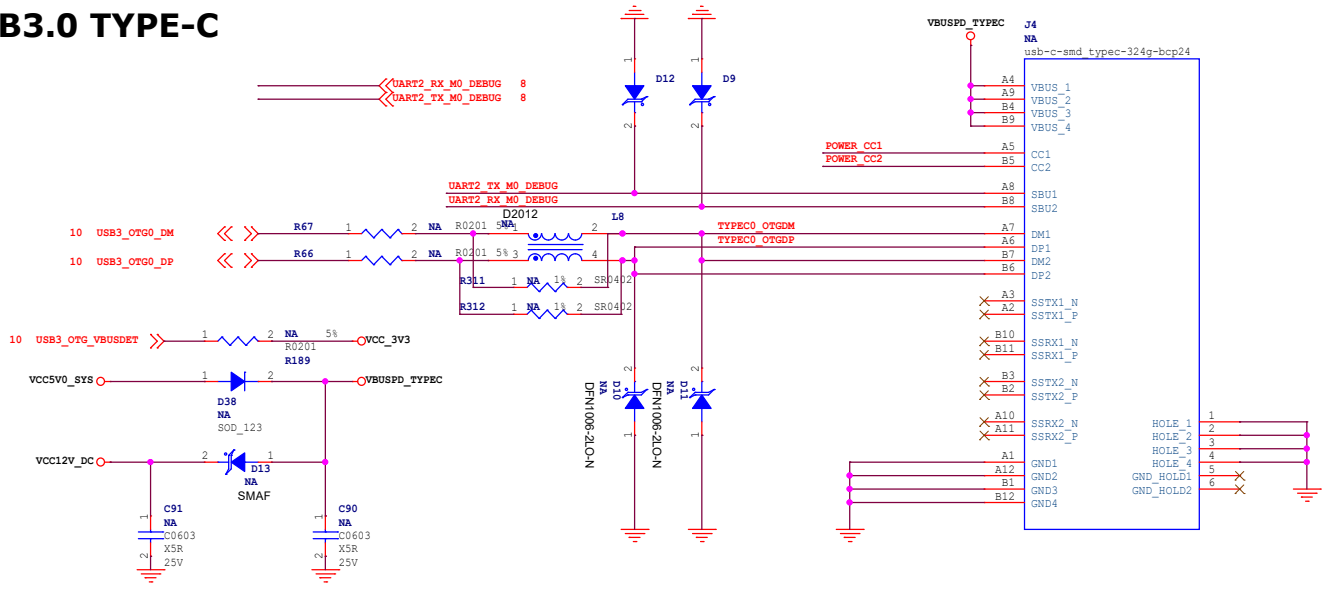
HINLINK

Project:	HNAS	
File:	20.Power_other	
Date:	Thursday, November 30, 2023	Rev: <Revision>
Designer:	<designer>	Sheet: 28 of 20

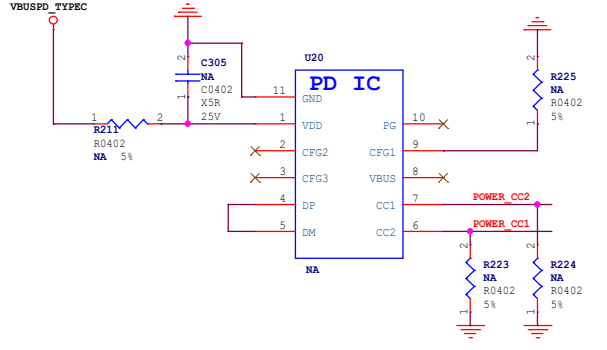
USB2.0 HOST PORT USB3.0 HOST PORT



USB3.0 TYPE-C



PD IC



HINLINK			
Project:	HNAS	Rev:	<Revision>
File:	21.USB2/USB3 Port	Rev:	<Revision>
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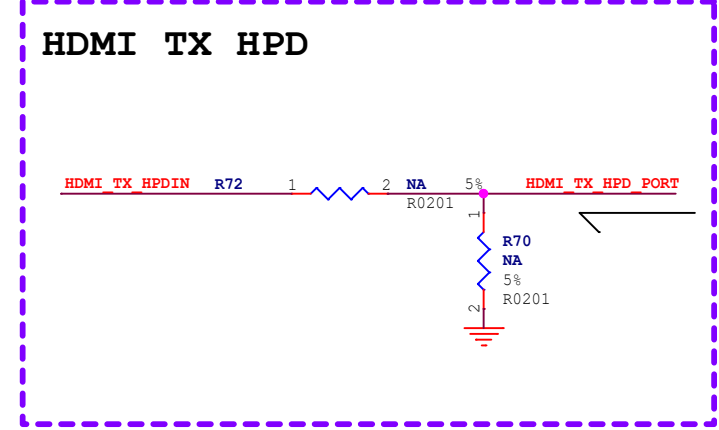
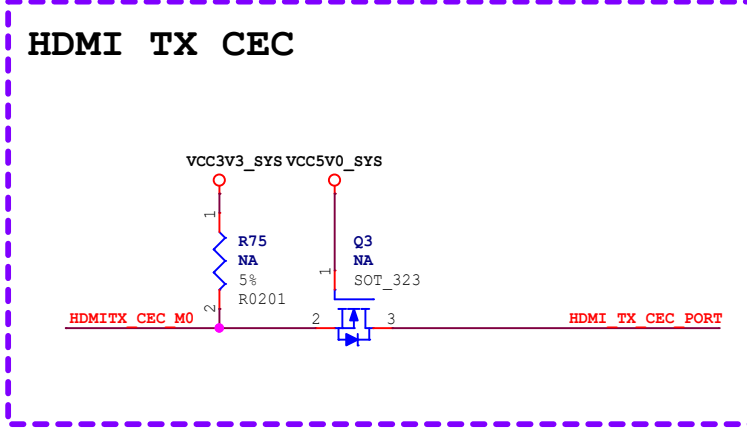
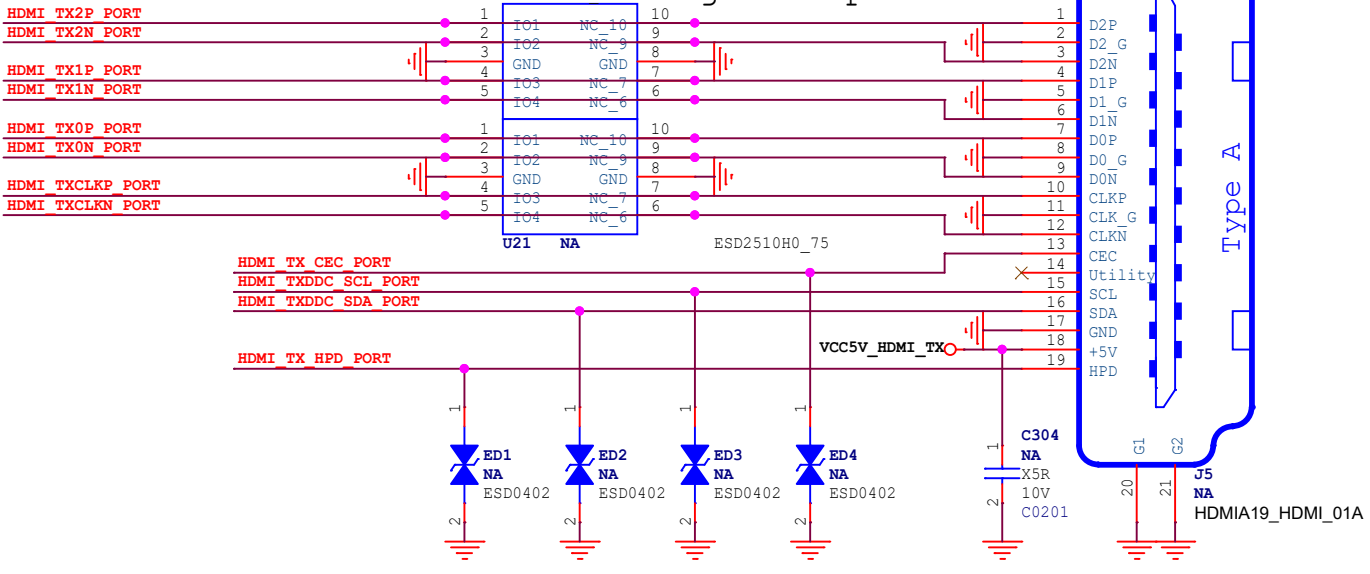
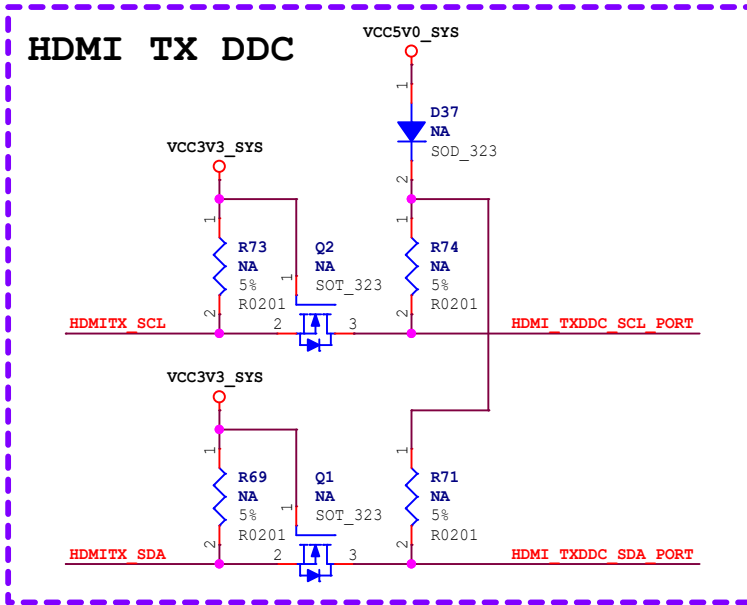
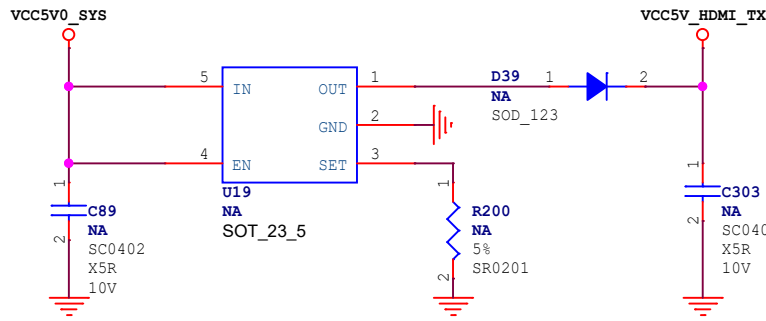
HDMI_TX2P_PORT >> HDMI_TX2P_PORT 13
 HDMI_TX2N_PORT >> HDMI_TX2N_PORT 13

 HDMI_TX1P_PORT >> HDMI_TX1P_PORT 13
 HDMI_TX1N_PORT >> HDMI_TX1N_PORT 13

 HDMI_TX0P_PORT >> HDMI_TX0P_PORT 13
 HDMI_TX0N_PORT >> HDMI_TX0N_PORT 13

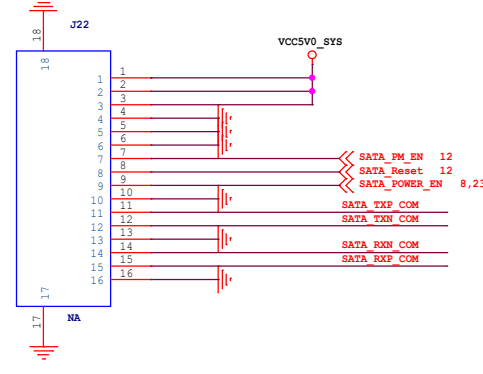
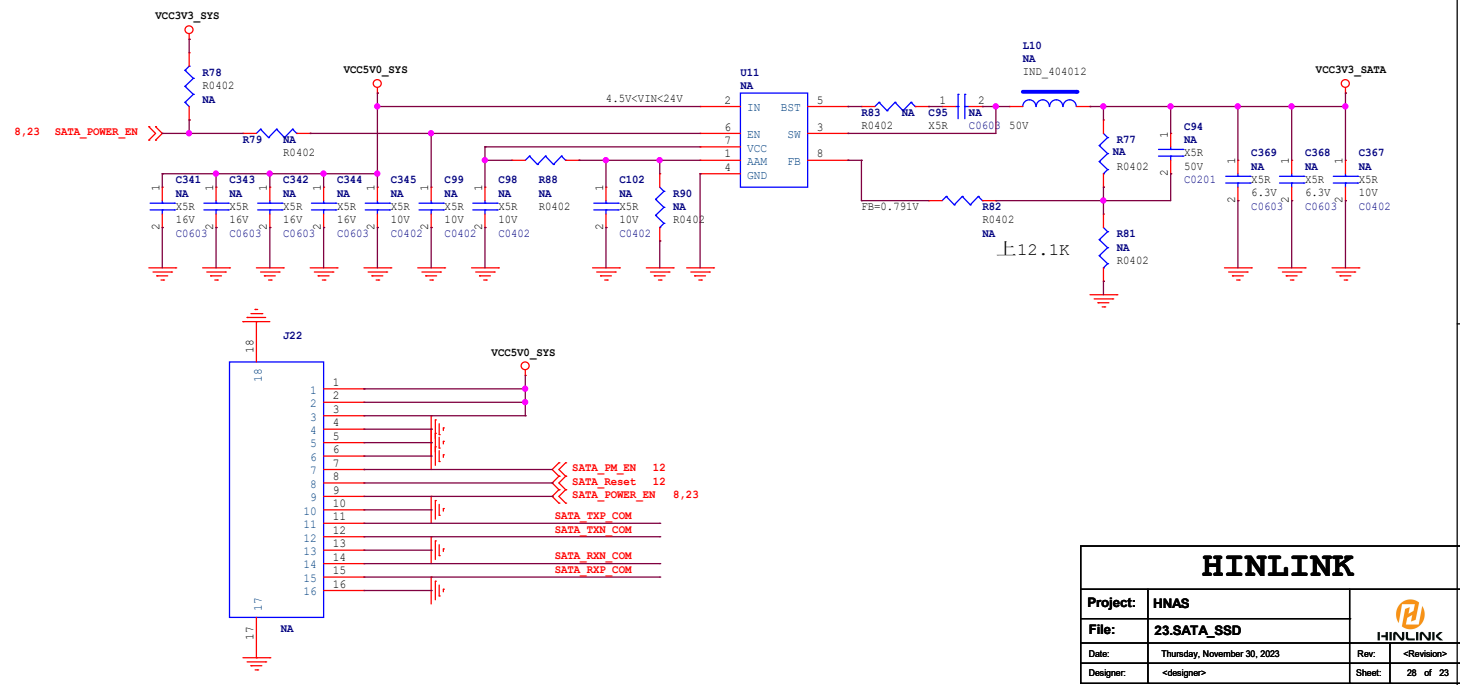
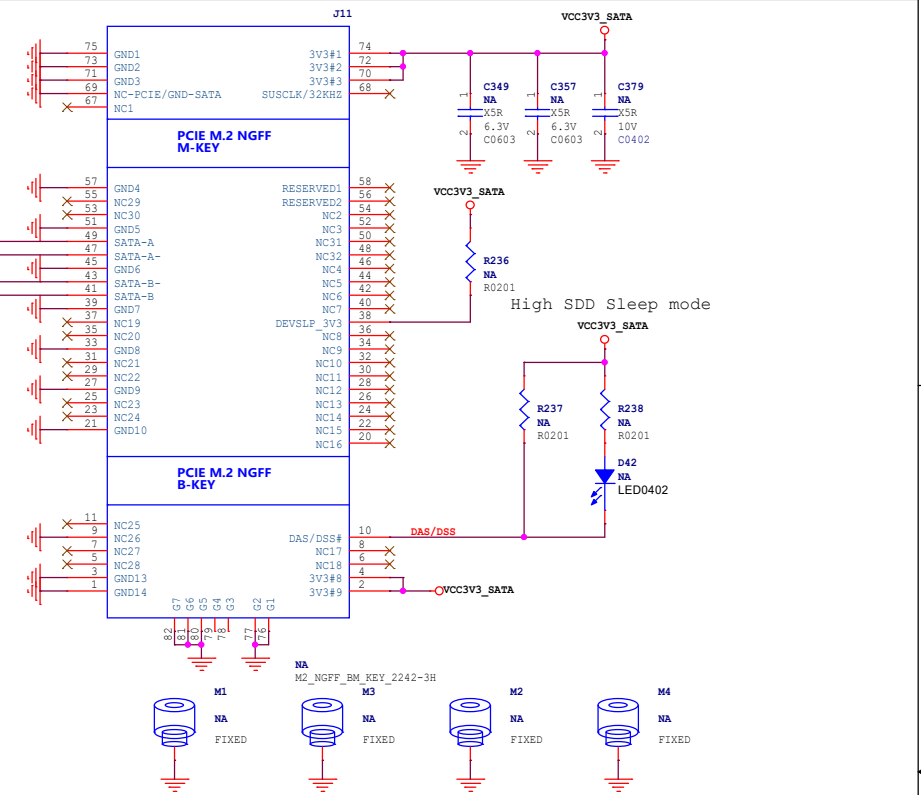
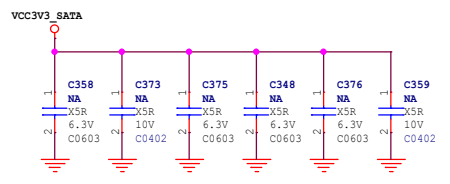
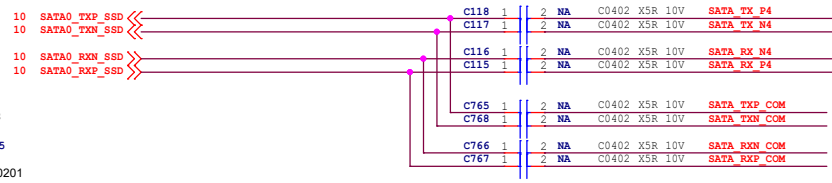
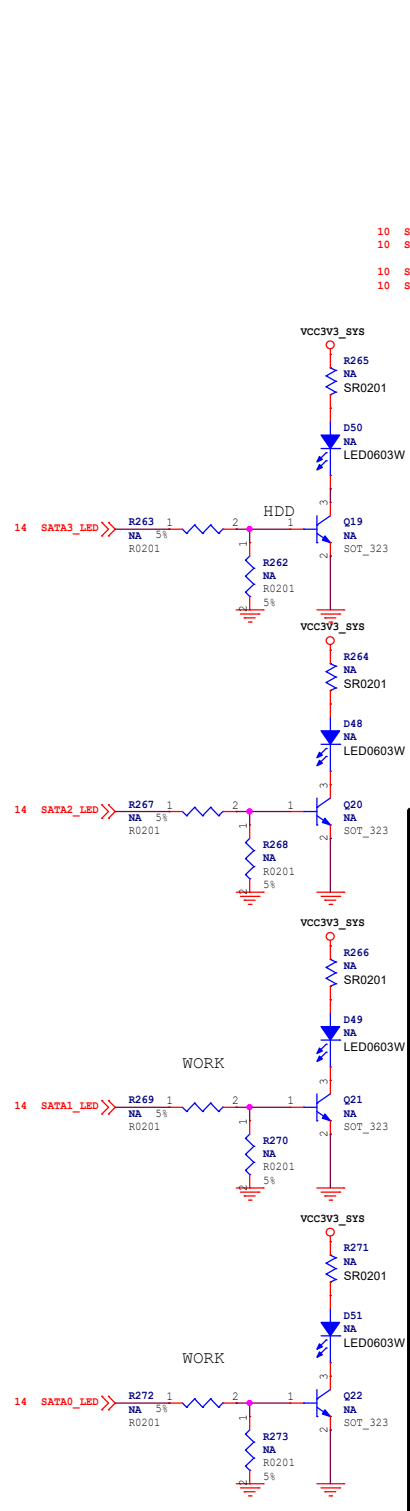
 HDMI_TXCLKP_PORT >> HDMI_TXCLKP_PORT 13
 HDMI_TXCLKN_PORT >> HDMI_TXCLKN_PORT 13

 HDMI_TX_SCL >> HDMI_TX_SCL 11
 HDMI_TX_SDA >> HDMI_TX_SDA 11
 HDMI_TX_CEC_M0 >> HDMI_TX_CEC_M0 11
 HDMI_TX_HPDIN >> HDMI_TX_HPDIN 13



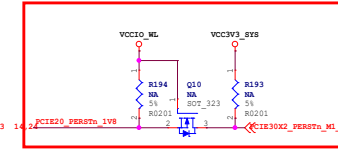
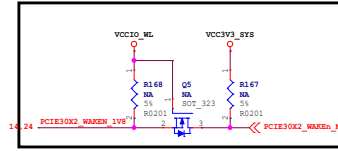
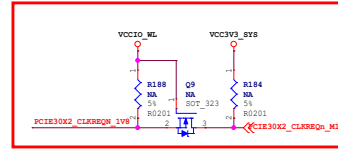
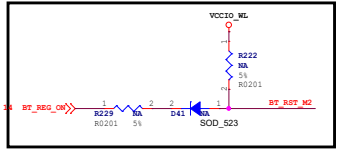
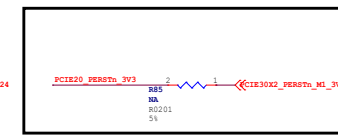
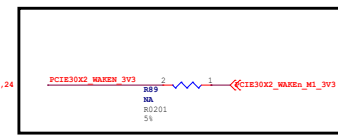
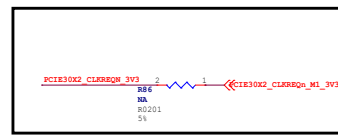
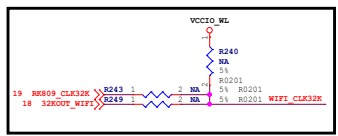
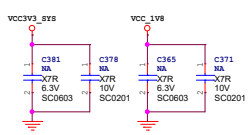
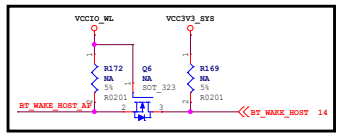
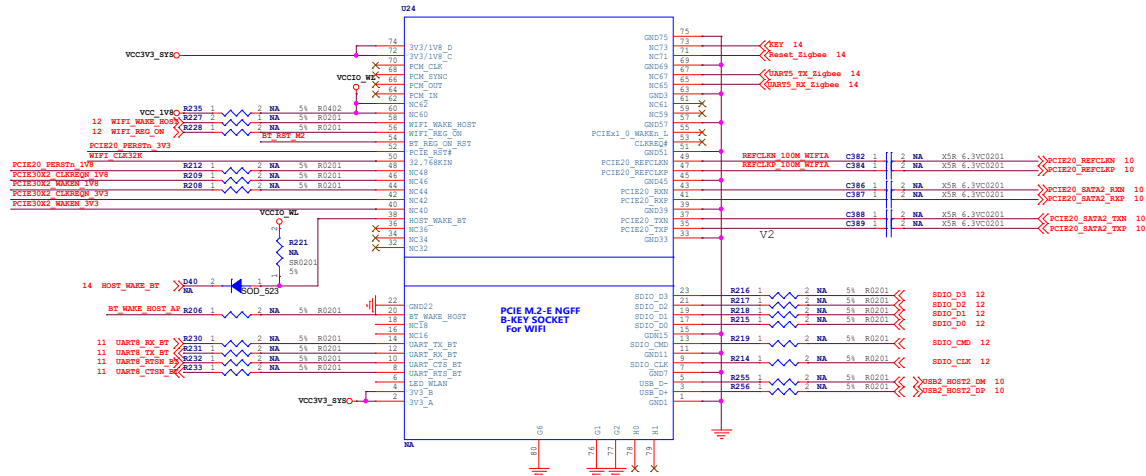
HINLINK		
Project:	HNAS	
File:	22.VO-HDMI2.0 TX	
Date:	Thursday, November 30, 2023	Rev: <Revision>
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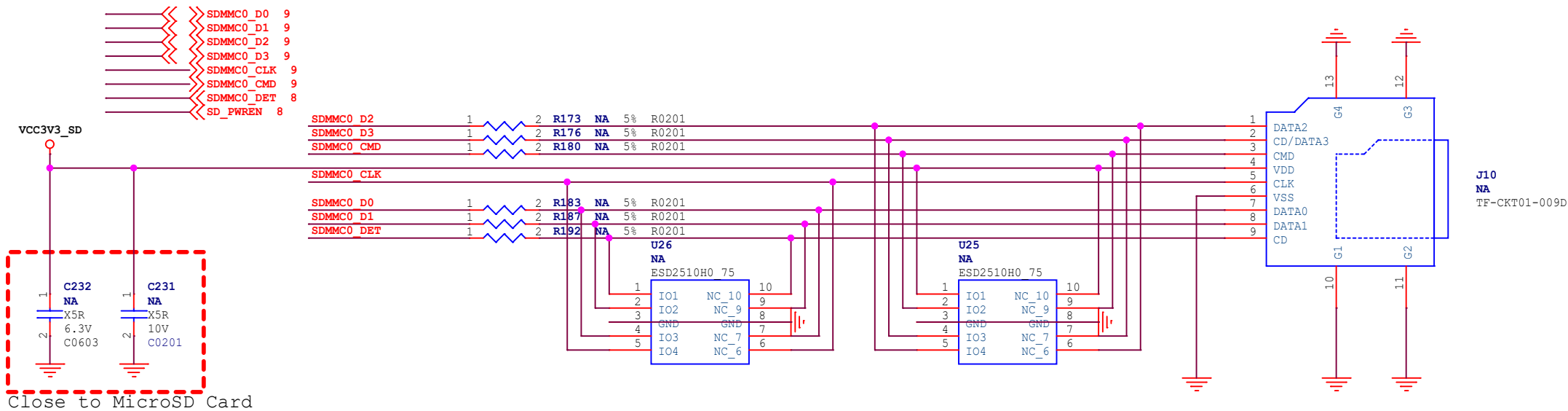
Rockchip Confidential



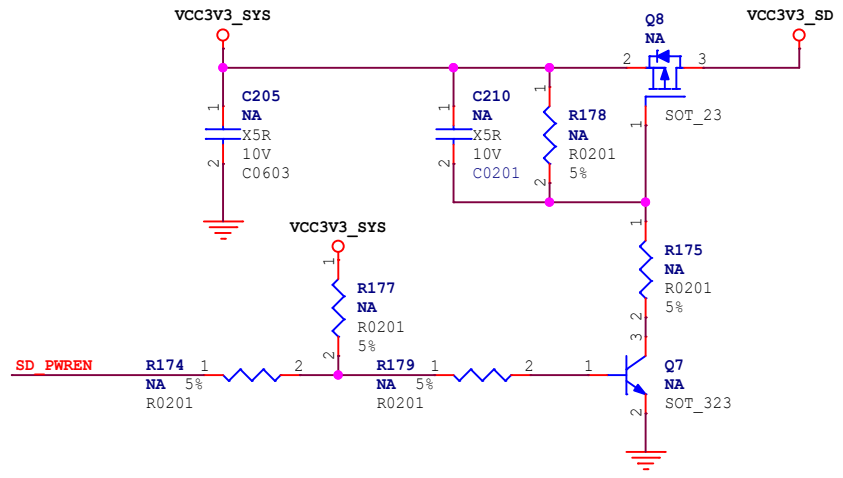
HINLINK			
Project:	HNAS		
File:	23.SATA_SSD		
Date:	Thursday, November 30, 2023	Rev:	<Revision>
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PCIe WIFI6/BT Module-2T2R



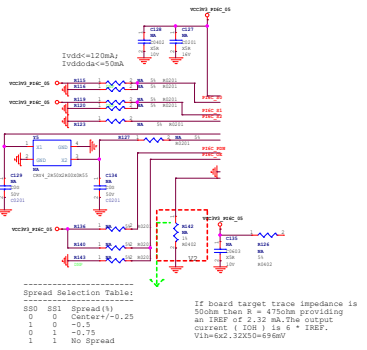


MicroSD Card

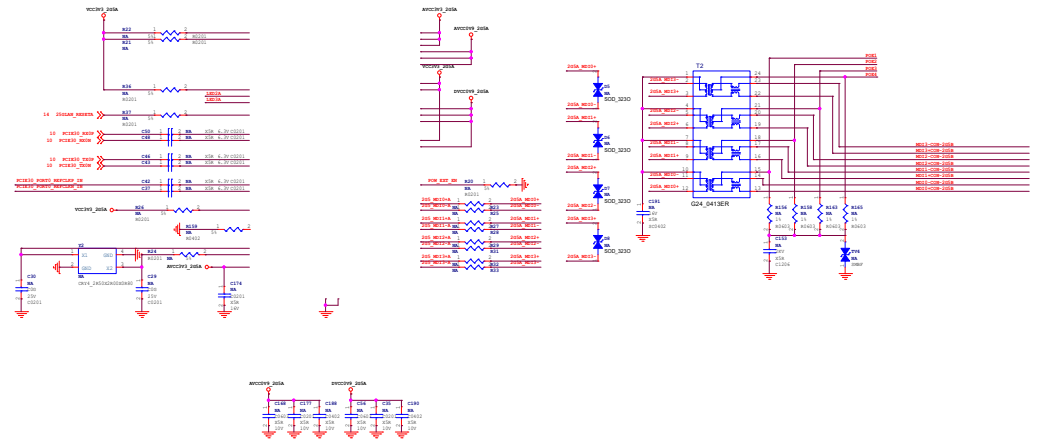


OWLVisionTech		
Project:	HNAS	 OWL Vision Tech
File:	25.Flash-MicroSD Card	
Date:	Thursday, November 30, 2023	Rev: <Revision>
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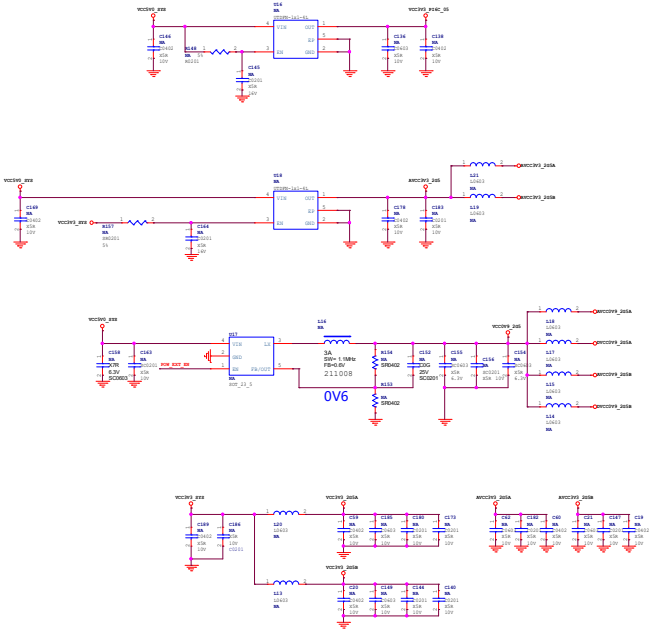
PCIe CLK Crystal Generator



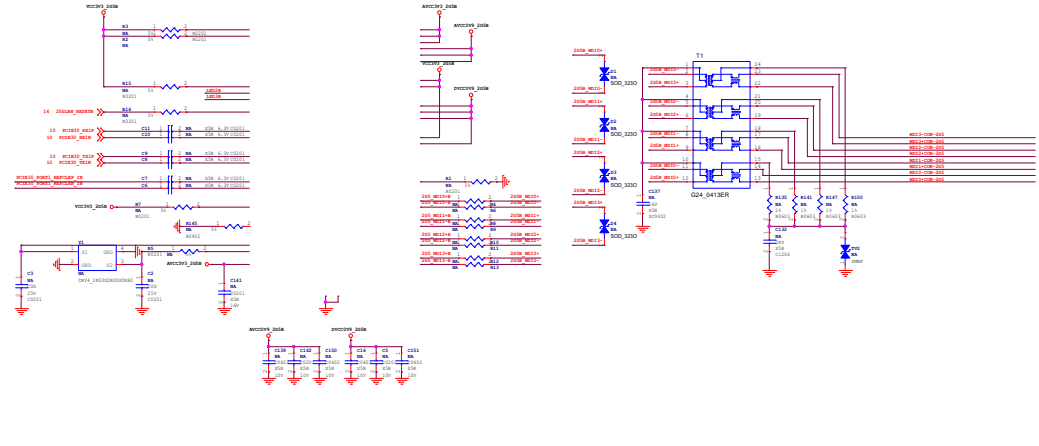
PCIe 2.5G A



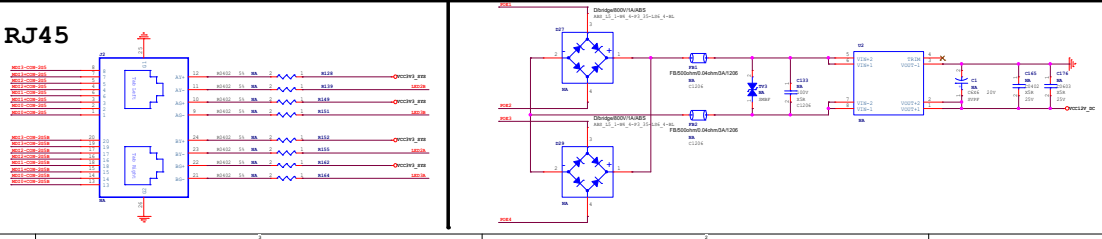
PCIe POWER

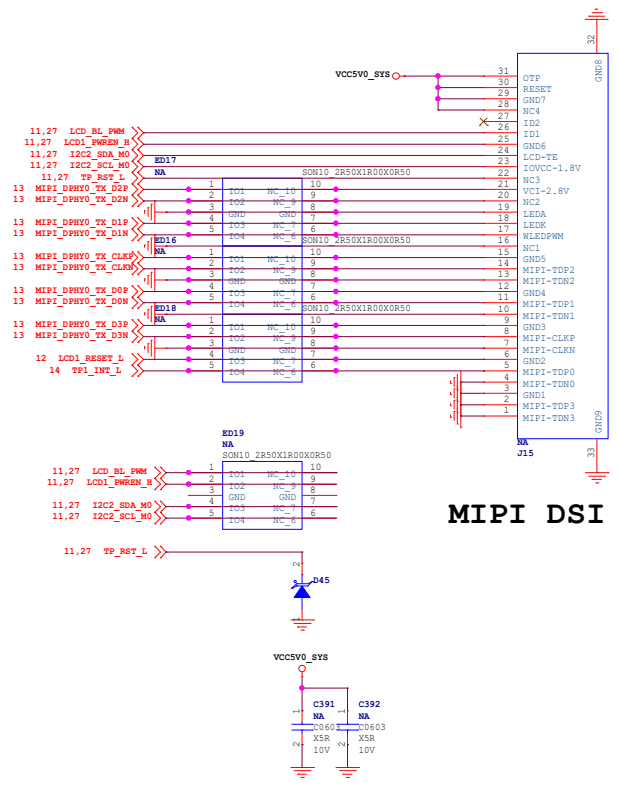


PCIe 2.5G B




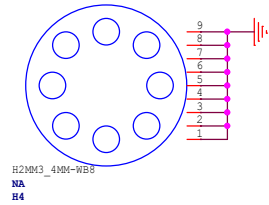
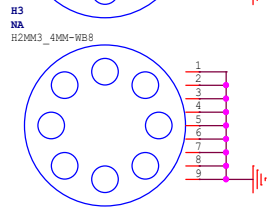
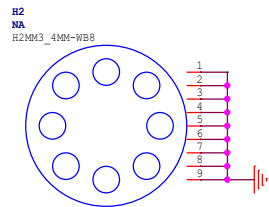
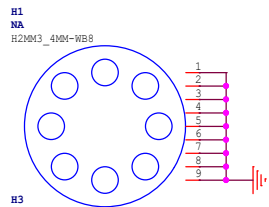
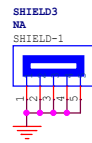
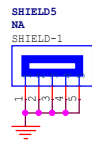
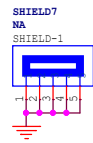
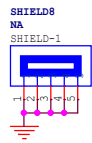
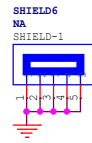
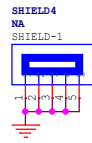
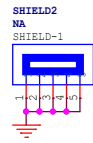
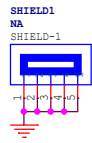
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MIPI DSI

HINLINK		
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HINLINK

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